ANALYSIS AND SIMULATION OF A CAPACITOR-DIODE VOLTAGE MULTIPLIER

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MASTER OF TECHNOLOGY

By

ATUL KUMAR

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

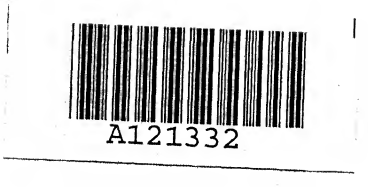
MARCH, 1995

CERTIFICATE

This is to certify that the thesis entitled, **"ANALYSIS AND SIMULATION OF A CAPACITOR-DIODE VOLTAGE MULTIPLIER"** by Atul Kumar has been carried out under my supervision and that it has not been submitted elsewhere for the award of a degree.

(Dr.AVINASH JOSHI)
PROFESSOR
DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY
KANPUR

March, 1995



ABSTRACT

Present work deals with the analysis of a capacitor - diode voltage multiplier. The full wave doubling rectifier has been chosen for this purpose. Analysis and simulation has been done for the rectifier fed by ideal and non ideal sine and square wave voltage sources. Analysis has also been done for the multiplier fed by ideal sine and square wave current sources. Later in the thesis, a modification has been suggested to the classical doubling rectifier circuit, in which the diodes have been replaced by switches.This has been done with a view to controlling the average output voltage. Also studied is the voltage doubling rectifier fed by a square wave voltage whose pulse width can be controlled.It is found that the average output voltage is not very sensitive to the variations in the pulse width of the square wave input voltage. Another scheme in which the classical doubling rectifier fed from PWM current and voltage sources, has been studied. Simulation results have been presented.

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to my supervisor Dr.Avinash Joshi for all his inspiration and encouragement, and his keen interest in the work. In spite of his busy schedule, he was available whenever I needed help.

Thanks are due to my colleagues Shesh Kumar, Tripta and Abhay for their help and suggestions. I am also thankful to my friends Sandeep, Sanjeev, Amit, Kukreja, Rajeev, Ali and Raman who always inspired me when the things were not that smooth. My thanks are also due to my cousins, Uncle and Auntie who encouraged me throughout my thesis work.

Finally my special thanks are due to my brother, sister and parents who supported me through their invaluable prayers. I am very grateful to them for their continual support and sacrifices which enabled me finish my work.

(ATUL KUMAR)

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INTRODUCTION

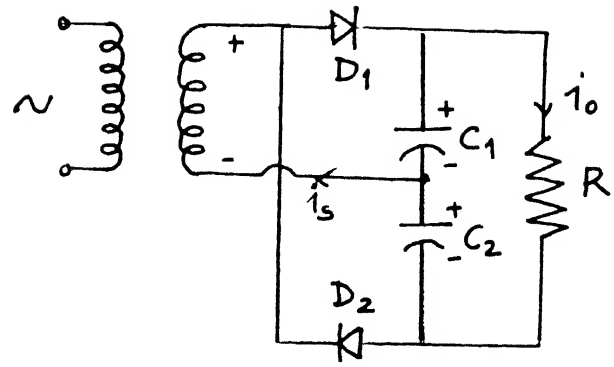
1.1 VOLTAGE MULTIPLIERS AND ITS APPLICATIONS - AN INTRODUCTION

Capacitor-diode voltage multipliers (CDVM) have been used in several applications as a simple and reliable means to obtain a high D.C voltage from an A.C source. Among the advantages offered by this solution is the fact that the a.c voltage may be substantially lower than the desired d.c voltage and that the capacitors and the diode ratings are lower too, as the sharing of the voltage stresses is intrinsically ensured by the multiplier operation.

When a transformer is used as an a.c source for the multiplier, substantial benefits in terms of voltage and insulation ratings of the transformer itself are obtained.

The CDVM advantages become particularly appreciable in those applications, such as space and communications, where small size and weight and high efficiency and reliability are of prime importance [4].In all these cases, the main disadvantage of CDVM, i.e., the delay between input and output and nonnegligible amount of capacitance needed, arereduced within acceptable limits by the increase of the operating frequency of today's converters.

In resonant converters, which are used more and more owing to the advantage of efficiency and the effects of parasitic



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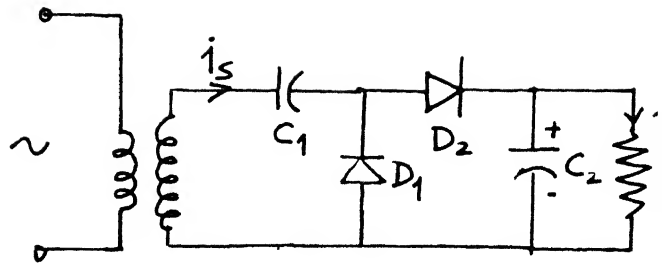

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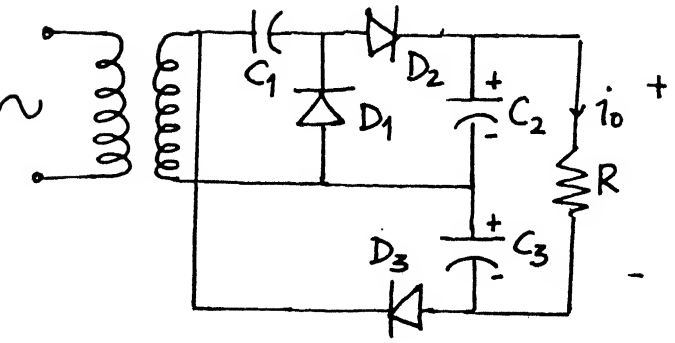

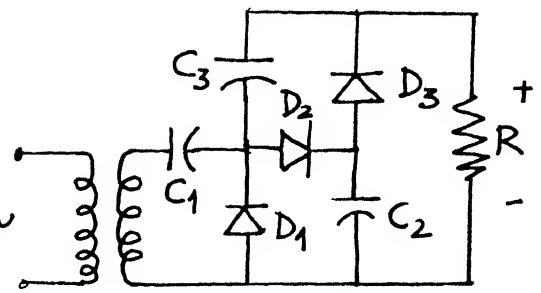

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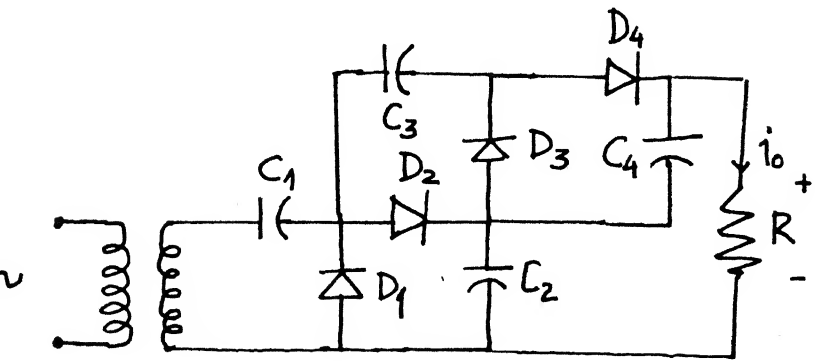

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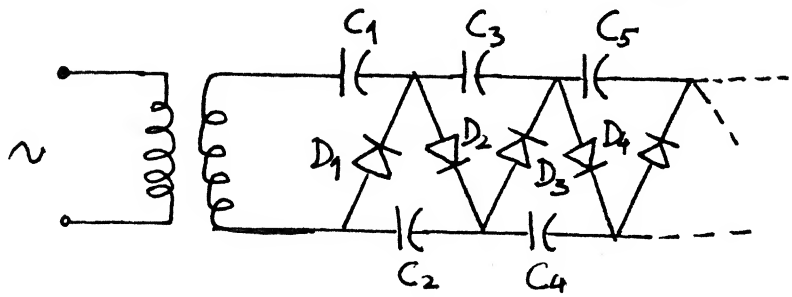


(e)

Fig.1.1 Typical Voltage Multiplier Circuits.

parameters they offer, the adoption of a voltage multiplier with a resonant converter may turn out to be very convenient.

There are many applications that require a well stabilised and regulated HV or EHT supply. Table 1.1 lists some of the important applications. In addition to all those listed in the table, HV supplies are used for image intensifier tubes, camera tubes, X-ray machines, insulatuion testers, and other specialised tubes and instruments.

1.2 METHODS TO PRODUCE HIGH VOLTAGE D.C.

a) To produce d.c output above 1kV it is possible to use a mains transformer with a secondary wound with the necessary number of turns, and this is the solution used in some oscilloscopes and X-ray systems where a simple fixed voltage unit at low cost is required. The drawbacks to this method are that the unit is rather bulky, the transformer and the smoothing capacitors required being very large, and the HV generated at the transformer secondary is highly dangerous since it has a relatively low impeadence. Smoothing capacitors in such units, because of their relatively high value, may also store a lethal charge for sometime after the mains is switched off.

b) Voltage Multilpliers circuits, of which there are several types, are very useful for producing high values of d.c voltage at low currents. Typical voltage multipliers are shown in Fig.1.1.

	Applications	Typical Current	Typical Voltage	Typical Regulation
1.	Cathode Ray Tubes used in oscilloscopes, radar displays and VDUs	A few milli amperes	2kV to 20kV	1%
2.	Photo multiplier tubes used in scintillating counter, flying spot scanners and low level photometery	0.5 mA to 5.0 mA	1kV to 3kV	0.1%
3.	Lamp supplies for photo copiers	5mA	5kV to 10kV	few percent

TABLE 1.1

The full wave doubling rectifier circuit (Fig.1.1a) is basically two half wave doubling rectifiers with the output summed by two capacitors. D_1 conducts on the positive half cycle to charge C_1 to E_m (the peak value of a.c secondary) and then on the negative half cycle D_2 conducts charge to C_2 also to E_m. As with other rectifiers of this type, the regulation is poor so that only a relatively light load of a few milli amperes can be supplied. Another doubler Fig.1.1(b) commonly used is also shown.

In this circuit C_1 must be a larger capacitance value than C_2. On negative half cycles, D_1 conducts and C_1 charges to E_m. On the next positive half cycle, the left plate of C_1 goes positive and D_2 conducts carrying C_2 to almost $2E_m$. Typically C_1 is twice the value of C_2 to allow correct charge sharing between the two capacitors. A voltage tripler can be constructed by adding an extra half wave rectifier as shown in Fig.1.1(c). Alternatively a tripler and quadrupler in Figl.1(d) can be made using a few sections of the well known Cockroft-Walton cascade rectifier Figl.1(e). Because the output impeadence of multipliers increases rapidly with the number of multiplier stages used, in most cases the rectifier in HV circuits is limited to a doubling rectifier circuit. The output impedance of the voltage multiplier increases approximately by the cube of the number of stages [5].A quadrupler has an output impedance about eight times greater than a doubling rectifier. High values of the output impedance limit the available output current and degrade the load regulation.

HV power units are specified in the same way as other d.c power supplies. Parmeters such as load and line regulation, output impedance, output ripple, temperature coefficient and stability being the most important.

In this thesis analysis and simulation has been done for a commonly used voltage multiplier circuit ,the full wave voltage doubling rectifier.

In chapter 2, analysis and simulation of a voltage doubling rectifier fed by ideal and non ideal sine wave voltage sources has been done. Differential equations were written and solved analytically for the rectifier fed by ideal sine wave. Differential equations for the doubling rectifier fed by non ideal sine wave voltage source are of second order and hence solved numerically. The numerical solutions have been obtained using a subroutine D02BAF from NAG library.

In chapter 3, analysis and simulation of the voltage doubling rectifier fed by ideal and nonideal square wave voltage source has ben done. Analytical solutions of the differential equations have been obtained for the former case. Numerical solutions have been obtained for the latter case using ,again, D02BAF subroutine from NAG library.

In chapter 4, analysis and simulation of a doubling rectifier fed by ideal sine and square wave current sources has been done. It has been found that the rectifier works as current halver.

Chapter 5 is devoted to SPICE simulation.In this cahpter, SPICE simulation of voltage doubling rectifier fed by a square wave whose pulse width can be controlled, has been done. This is done with a view to controlling the output voltage. Also studied is the voltage doubling rectifier fed by PWM voltage and current sources. A modification has been suggested to the classical voltage doubling rectifier. As per this modification, the diodes have been replaced by switches.This modified doubling rectifier is found to generate controlled output voltage when fed from a square wave voltage source of a constant pulse width.

CHAPTER 2

VOLTAGE DOUBLING RECTIFIER FED BY SINE WAVE VOLTAGE SOURCES

In this chapter analysis and simulation of the voltage doubling rectifier fed by ideal and nonideal sinusoidal voltage sources has been done. Simulation results have been discussed.Some important conclusions have been made.

2.1 VOLTAGE DOUBLING RECTIFIER FED BY AN IDEAL SINEWAVE VOLTAGE SOURCE

The doubling rectifier (Fig.2.1) with ideal sinusoidal supply has three modes of operation. These modes are characterised by the patterns of diode conduction. The mode transitions are shown in Fig.2.2. The modes are:

Mode 1 :D_1 ON , D_2 OFF, $\alpha < \omega t \leq \beta$

Mode 2 :D_1 OFF, D_2 OFF, $\beta < \omega t \leq \pi + \alpha$ and $\pi + \beta < \omega t \leq 2\pi + \alpha$

Mode 3 :D_1 OFF, D_2 ON , $\pi + \alpha < \omega t \leq \pi + \beta$

The description of each mode is as follows:

Mode 1: In this mode the diode D_1 conducts as supply voltage is larger than capacitor voltage , V_{c1} at $\omega t = \alpha$. The equivalent circuit for this mode is shown in Fig.2.3 . At $\omega t = \beta$, diode D_1 goes off as the source current, i_s becomes zero and circuit transits to Mode 2. Diode D_2 always remains off throughout this mode as the voltage across its anode to cathode never becomes positive. The voltage across capacitor 1 is same as the supply voltage.

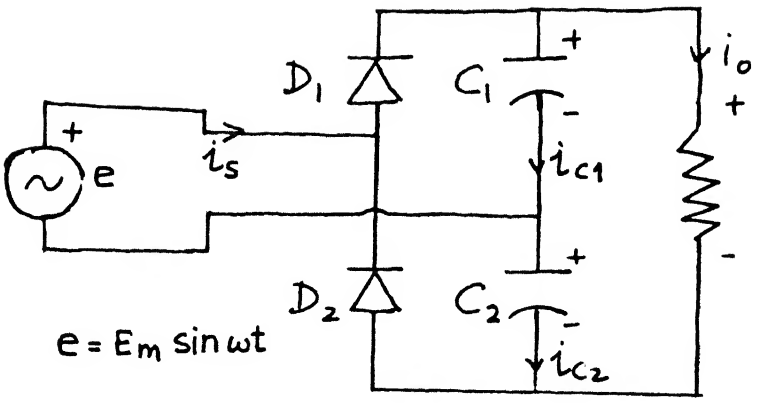


Fig.2.1(a) Voltage Doubling Rectifier fed by an ideal sine wave voltage source.

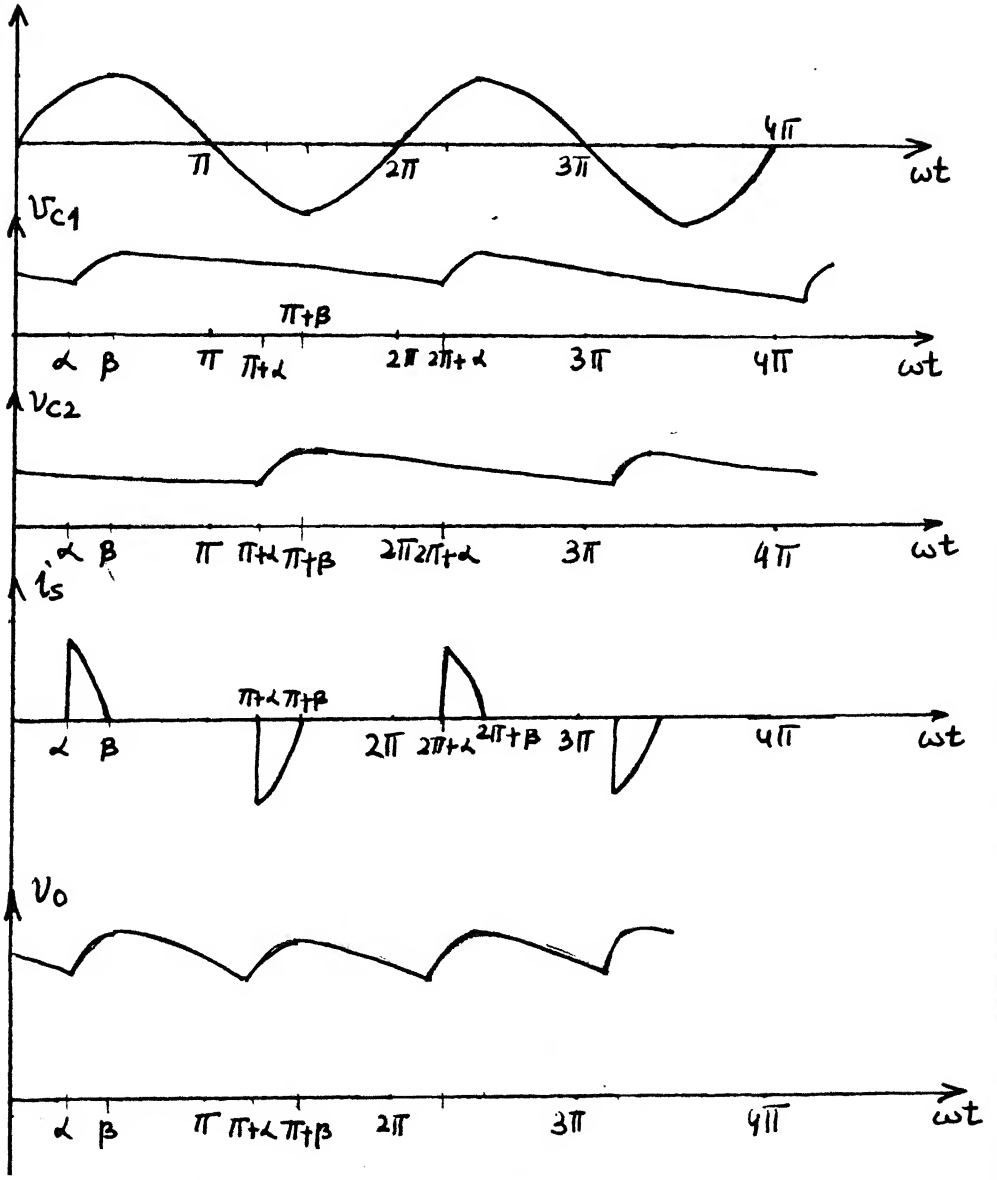


Fig.2.1(b) Typical Circuit Waveform for the circuit of Fig.2.1(a).

Mode 2: In this mode both diodes D_1 and D_2 are off and current supplied by source is zero. Voltage from anode to cathode for both the diodes remains negative throughout this mode . At $\omega t = \pi + \alpha$, the voltge across diode D_2 becomes positive and this diode turns on.The circuit transits to Mode 3. The equivalent circuit for Mode 2 is given in Fig.2.4. Load is supplied by energy stored in capaciotors C_1 and C_2.

Mode 3: In this mode the diode D_2 conducts as the negative of supply voltage is larger than capacitor voltage , V_{c2} at $\omega t = \pi + \alpha$ .The equivalent circuit for this mode is shown in Fig.2.5 . The voltage across capacitor 1 falls . The voltage across capacitor 2 is same as the negative of the supply voltage.At $\omega t = \pi + \beta$, diode D_2 goes off for the source current,i_s becomes equal to zero and the circuit transits to Mode 2 again .The diode D_1 remains off throughout this period from $\omega t = \pi + \alpha$ to $\pi + \beta$ as the voltage across its anode to cathode remains negative . The circuit remains in Mode 2 till $\omega t < 2\pi + \alpha$ and at $\omega t = 2\pi + \alpha$ the circuit transits to Mode 1 again and the same proces repeats . Cyclic change in the modes of operation is given in Fig.2.2 . The pattern of modes in steady state is 1,2,3,2,1,.. . The typical wave-forms of V_{c1}, V_{c2}, i_s in steady state are shown in Figs. 2.1(b).

2.1.1 DIFFERENTIAL EQUATIONS OF THE VOLTAGE DOUBLING RECTIFIER FOR MODES 1,2,3 AND THE METHOD OF SOLUTION

In this section the differential equations describing the

rectifier in different modes have been derived . The equations are solved for the expressions for voltage across capacitor 1, $V_{c1}(t)$, voltage across capacitor 2 , $V_{c2}(t)$. The two variables of interest are V_{c1} and V_{c2} in this circuit . The reference directions for capacitor voltages and currents are shown in Fig.2.1(a) . KVL and KCL have been applied to derive the differential equations . The diodes D_1 and D_2 are assumed to be ideal.

NORMALISATION SCHEME : The sinusoidal voltage source applied is $E_m \sin\omega t$. The amplitude E_m is taken as base voltage . Base impedance is $1/\omega C$. The base current thus becomes $E_m.\omega.C$. Normalised load ressistance as per this scheme becomes $\omega.C.R$. The equations derived for V_{c1}, V_{c2}, i_s have been converted in p.u.form using above normalisation scheme. This normalisation scheme helps to obtain design relations for the power doubling rectifier . All normalised variables are indicated by suffix n e.g. i_{sn} is the normalised source current .

Mode 1 (Fig. 2.3): In this mode D_1 is on and D_2 is off .Source current is positive . The circuit enters Mode 1 at $\omega t = \alpha$. The three differential equations are :

$$\text{source current}, i_s = C.E_m.\omega.\cos(\omega t) + (V_{c1} + V_{c2})/R \quad [2.1]$$

$$\text{capacitor 1 voltage }, V_{c1} = E_m.\sin(\omega t) \quad [2.2]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c2})/dt \quad [2.3]$$

Equations 2.2 and 2.3 give

$$(1/R.C.+ D)V_{c2} = -(E_m/RC).\sin(\omega t) \quad [2.4]$$

where $D \equiv d/dt$

Solution of above differential equation yields

$$V_{c2} = -(E_m)/(1 + \omega^2.R^2.C^2) .\sin(\omega t) + K_1.\exp(-t / RC) + (E_m.\omega.R.C)/(1 + \omega^2.R^2.C^2) .\cos(\omega t) \quad [2.5]$$

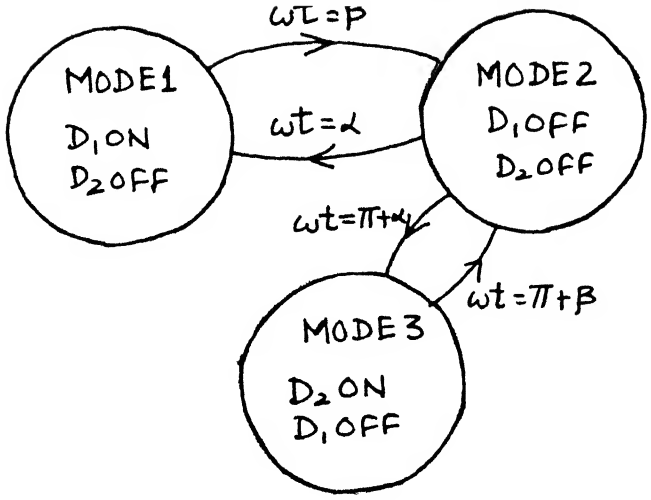


Fig.2.2 Mode Transition diagram for the Voltage Doubling Rectifier fed by ideal sine wave voltage source

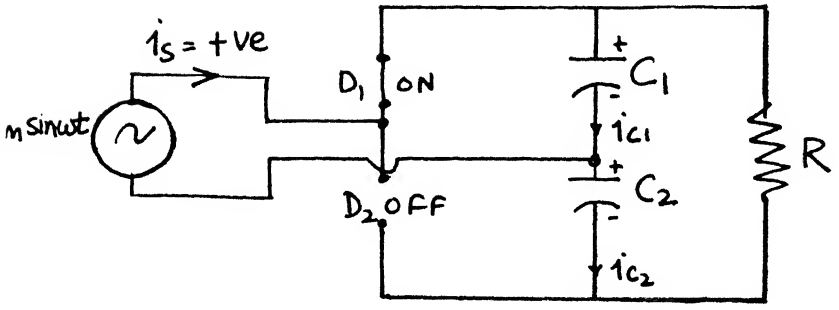


Fig.2.3 Equivalent circuit in Mode 1

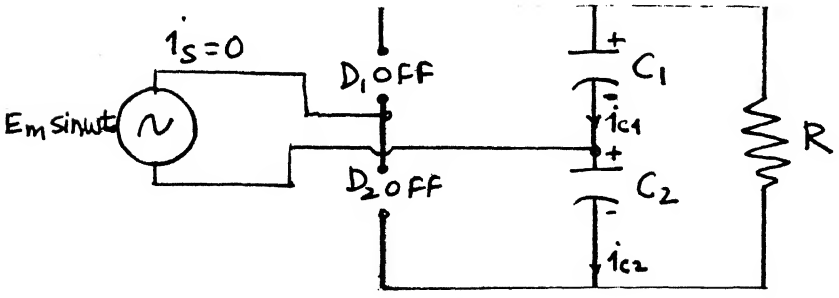


Fig.2.4 Equivalent circuit in Mode 2.

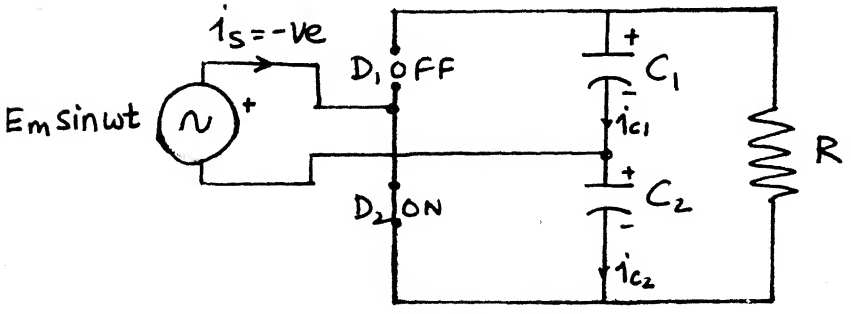


Fig.2.5 Equivalent circuit in Mode 3.

Applying the initial conditions,

$\omega t = \alpha$, $V_{c2} = V_{c2}(\alpha)$ in eq. 2.5, we have

$$K_1 = [\, V_{c2}(\alpha)^{*} + E_m.\sin(\alpha)/(\, 1 + \omega^2.R^2.C^2)].\exp(\, \alpha \,/\, \omega.R.C)$$

$$- [\, E_m.\omega.R.C.\cos(\alpha) \,/\, (1 + \omega^2.R^2.C^2)].\exp(\, \alpha \,/\, \omega.R.C) \qquad [2.6]$$

Normalised equations (as per normalisation scheme given above) for voltage across capacitor 1, voltage across capacitor 2 and source current ,i_s are given below :

$$V_{c1n} = \sin(\omega t) \qquad [2.7]$$

$$V_{c2n} = p1.\sin(\omega t) + p2.\cos(\omega t) + k_{1n}.\exp(-\omega t/R_n) \qquad [2.8]$$

$$i_{sn} = \cos(\omega t) + (V_{c1n} + V_{c2n})/R_n \qquad [2.9]$$

where R_n , p1 , p2 and k_{1n} are given by

$$R_n = \omega.R.C$$

$$p1 = -1/(R_n^2 + 1)$$

$$p2 = R_n/(R_n^2 + 1)$$

$$k_{1n} = k_1/E_m$$

Equations 2.4 , 2.5 and 2.6& 2.7 , 2.8 and 2.9 describe the operation of doubling rectifier in Mode 1.

Mode 2 (Fig. 2.4) : This mode is characterized by the condition that both diodes are off and as a result source current i_s is zero . This mode starts at $\omega t = \beta$ .The three equations are as follows :

$$\text{source current , } i_s = 0 \qquad [2.10]$$

$$\text{capacitor 1 voltage , } V_{c1} = V_{c1}(\beta).\exp(-2/RC)(t-\beta/\omega) \qquad [2.11]$$

$$\text{capacitor 2 voltage , } V_{c2} = V_{c2}(\beta)^{*}.\exp(-2/RC)(t-\beta/\omega) \qquad [2.12]$$

where $V_{c1}(\beta) = E_m.\sin(\beta)$ (From Eq. 2.2)

Normalised equations are given below

$$V_{c1n} = \sin(\beta).\exp(-2/R_n)(\omega t-\beta) \quad [2.13]$$

$$V_{c2n} = V_{c2}(\beta)/E_m.\exp(-2/R_n)(\omega t-\beta) \quad [2.14]$$

$$i_{sn} = 0 \quad [2.15]$$

Equations 2.10, 2.11 and 2.12 & 2.13, 2.14 and 2.15 describe the doubling rectifier in Mode 2 .

Mode 3 (Fig. 2.5) : This mode is characterized by the condition that diode D_2 is on and diode D_1 is off .In other words source current i_s is negative .This mode starts at $\omega t = \pi + \alpha$. The three equations for this mode are given below :

capacitor 2 voltage ,$V_{c2} = -E_m.\sin(\omega t)$ [2.16]

source current , $i_s = C.E_m.\omega.\cos(\omega t) - (V_{c1} + V_{c2})/R$ [2.17]

$(V_{c1} + V_{c2})/R = -C.d(V_{c1})/dt$ [2.18]

Equations 2.16 and 2.18 give ,

$$V_{c1} = E_m/(1 + \omega^2R^2C^2).[\sin(\omega t)-\omega^2R^2C^2.\cos(\omega t)] + K_2.\exp(-t/RC) \quad [2.19]$$

* see Appendix 1 for derivation of the expression for $V_{c2}(\alpha)$

Applying the initial conditions , $\omega t = \pi + \alpha$, $V_{c1} = V_{c1}(\pi + \alpha)$ in Eq. 2.19 , we have

$$K_2 = V_{c1}(\pi + \alpha)^{*} + E_m/(1+\omega^2R^2C^2)\{\sin(\alpha)-\omega^2R^2C^2.\cos(\alpha)\}.\exp(\pi + \alpha)/\omega^2R^2C^2 \quad [2.20]$$

Normalised equations for V_{c1} , V_{c2} and i_s are given below :

$$V_{c1n} = 1/(1+R_n^2)[\sin(\omega t)-R_n.\cos(\omega t)] + K_{2n}.\exp(-\omega t/R_n) \quad [2.21]$$

$$V_{c2n} = -\sin(\omega t) \quad [2.22]$$

$$i_{sn} = \cos(\omega t) - (V_{c1n} + V_{c2n})/R_n \quad [2.23]$$

where $k_{2n} = k_2/E_m$

Equations 2.16 , 2.17 and 2.18 & 2.21 , 2.22 and 2.23 describe

Method of solution : The equations for different modes derived above have been programmed on HP 9000 using Fortran 77.The flow charts of the program are shown in Fig. 2.6.The transient behaviour has been calculated from zero initial conditions and steady state has been obtained after a no. of cycles.The initial conditions $V_{c2}(\alpha)$,$V_{c2}(\beta)$ and $V_{c1}(\pi+\alpha)$ have been calculated and given in Appendix 1.

2.1.2.AVERAGE OUTPUT VOLTAGE

In this section an expression for average output voltage has been derived .The average output voltage is calculated over one half period i.e.π radians.The output voltage repeats every π radians i.e.the frequency of the ripple in the output voltage is twice the frequency of input supply . The expression for the output voltage has ,thus ,been derived by integrating $V_{c1} + V_{c2}$ from α to $\Pi + \alpha$ in two intervals , α to β and β to $\pi + \alpha$.

$$\text{Average output voltage ,Vo} = 1/\pi \left[\int_{\alpha}^{\pi+\alpha} (V_{c2} + V_{c1}).d(\omega t) \right]$$

$$= 1/\pi \left[\int_{\alpha}^{\beta} (V_{c1}+V_{c2})d(\omega t) + \int_{\beta}^{\pi+\alpha} (V_{c1}+V_{c2})d(\omega t) \right]$$

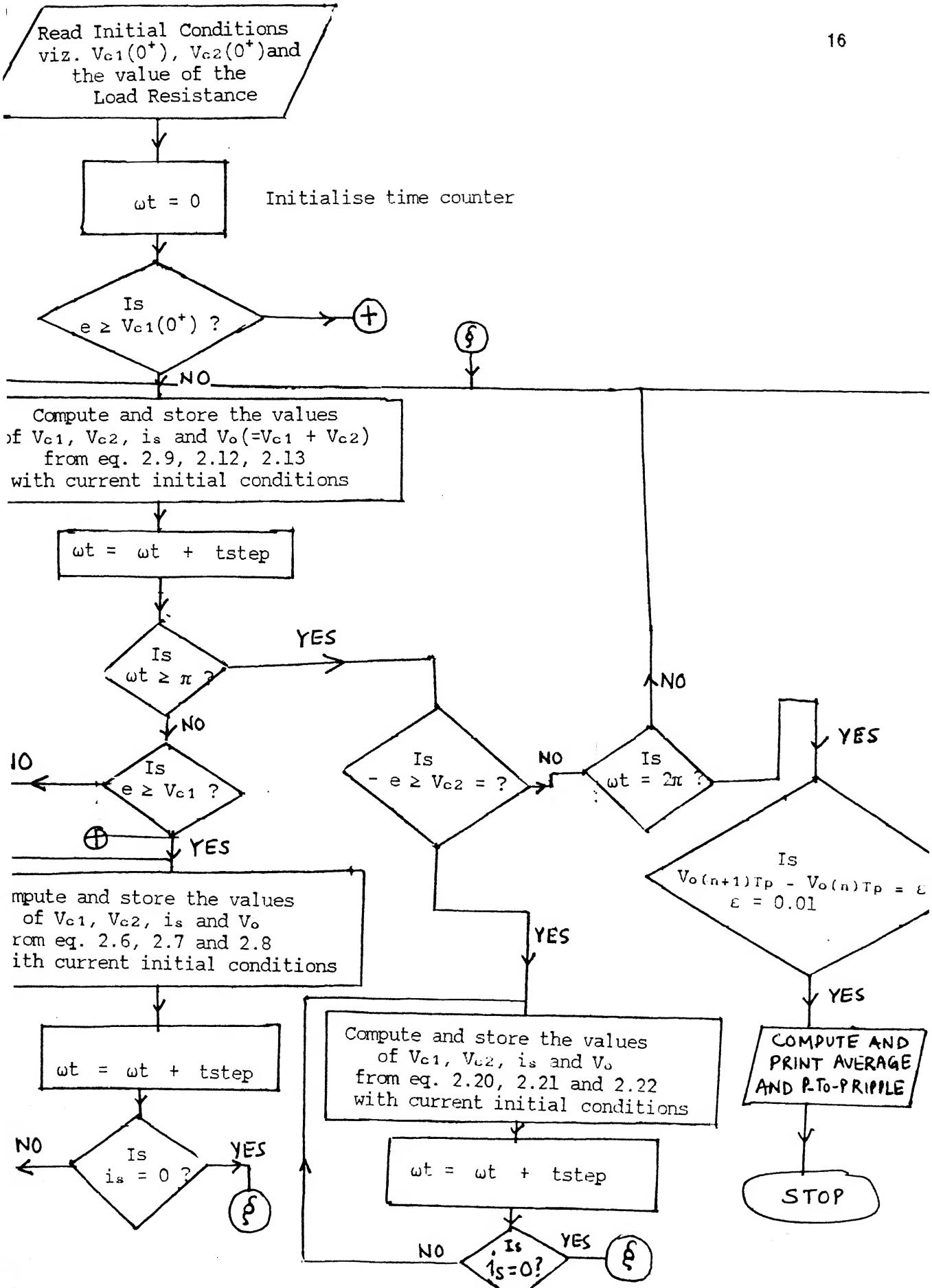
[2.24]

Substituting for V_{c1} ,V_{c2} from equations 2.2 , 2.5 , 2.11 and 2.12 in 2.24 suitably , we get

$$Vo = 1/\pi \{ A + B + C + D\} \qquad [2.25]$$

where $$A = E_m.[\cos(\alpha)-\cos(\beta)] \qquad [2.26]$$

$$B = R_n/2.E_m.\sin(\beta).[1 - \exp(2\beta-2\alpha-2\pi)/\omega^2R^2C^2 \qquad [2.27]$$


Read Initial Conditions viz. $V_{c1}(0^+)$, $V_{c2}(0^+)$ and the value of the Load Resistance
$\omega t = 0$
Initialise time counter
Is $e \geq V_{c1}(0^+)$?
NO
Compute and store the values of V_{c1}, V_{c2}, i_s and $V_o (= V_{c1} + V_{c2})$ from eq. 2.9, 2.12, 2.13 with current initial conditions
$\omega t = \omega t + tstep$
Is $\omega t \geq \pi$?
YES
NO
Is $e \geq V_{c1}$?
YES
mpute and store the values of V_{c1}, V_{c2}, i_s and V_o rom eq. 2.6, 2.7 and 2.8 ith current initial conditions
$\omega t = \omega t + tstep$
Is $i_s = 0$?
NO
YES
Is $-e \geq V_{c2}$ = ?
NO
YES
Compute and store the values of V_{c1}, V_{c2}, i_s and V_o from eq. 2.20, 2.21 and 2.22 with current initial conditions
$\omega t = \omega t + tstep$
Is $i_s = 0$?
NO
YES
Is $\omega t = 2\pi$?
NO
YES
Is $V_{o(n+1)Tp} - V_{o(n)Tp} = \varepsilon$
$\varepsilon = 0.01$
YES
COMPUTE AND PRINT AVERAGE AND P-TO-PRIPPLE
STOP

$$C = p1.E_m.[\cos(\alpha)-\cos(\beta)]+p2.E_m.[\sin(\beta)]$$
$$- p2.E_m.[\sin(\alpha)]-K_1.\omega^2R^2C^2.[\exp(-\beta/\omega^2R^2C^2)-\exp(-\alpha/\omega^2R^2C^2)] \quad [2.28]$$

$$D = \omega^2R^2C^2/2.V_{c2}(\beta).[1-\exp(2\{\alpha+\pi\}-2\beta)/\omega^2R^2C^2] \quad [2.29]$$

$$V_{on} = V_o / E_m = (1/\pi).E_m.(A + B + C + D)$$

$$I_{on} = V_{on}/R_n$$

Derivations of expressions for A,B,C and D are given in Appendix 1

2.1.3. PEAK TO PEAK OUTPUT VOLTAGE RIPPLE

In this section an expression for peak to peak output voltage ripple has been derived. The output voltage follows a certain pattern .It reaches maximum at $\omega t = \beta$ and touches the lowest point at $\omega t = \alpha$. This is the period when diode D_1 is on and D_2 is off . The same voltage ripple is observed during the period from $\omega t = \pi + \alpha$ to $\omega t = \pi + \beta$, the period during which diode D_2 is on D_1 is off.Hence peak to peak voltage ripple is calculated during this period only.

$$V_{ripple(p-p)} = (Vo)_{\omega t=\beta} - (Vo)_{\omega t=\alpha}$$
$$V_{ripple(p-p)} = (V_{c1}+V_{c2})_{\omega t=\beta} - (V_{c1}+V_{c2})_{\omega t=\alpha}$$

Equations 2.2 and 2.5 in 2.31 give

$$V_{ripple(p-p)} = E_m.\sin(\beta) + [E_m.\omega.R.C./(1+\omega^2R^2C^2).\cos(\beta)] +$$
$$[K_1.\exp(-\beta/\omega.R.C)]- E_m/(1+\omega^2R^2C^2).\sin(\beta) - E_m.\sin(\alpha) - V_{c2}(\alpha) \quad [2.31a]$$

Normalisation gives

$$V_{ripple(p-p)n} = \sin(\beta)+ [R_n/(1+R_n^2).\cos(\beta)] + [K_{1n}.\exp(-\beta/R_n)]$$
$$- 1/(1+R_n^2).\sin(\beta) - \sin(\alpha) - V_{c2n}(\alpha) \quad [2.31b]$$

The expression for peak to peak voltage ripple in original and normalised form could be used for design purposes.

2.1.4.DISCUSSION OF SIMULATION RESULTS

In this section the general behaviour of the doubling rectifier has been studied . The transient behaviour,steady state behaviour,average output voltage and peak to peak voltage ripple for different values of load resistances have been calculated and shown in Figs.2.7, 2.8 and 2.9.These results are discussed below :

2.1.4.1 Loaded Transient and Steady State Behaviour

Fig. 2.7 shows the simulated output voltage,voltage across capacitor 1, voltage across capacitor 2,source current i_s and input voltage for the doubling rectifier with load resistance of 10.0 p.u.

The circuit of figure 2.1 is excited from cold and its transient behaviour is noticed . At $\omega t=0^+$, diode D_1 turns on as the supply voltage is larger than voltage across capacitor 1 (being 0).This allows the capacitor to follow the supply voltage (the circuit is in Mode 1 where $V_{c1n} = \sin(\omega t)$) .The voltage across capacitor 2 increases in the negative direction(see Fig 2.3).The circuit remains in Mode 1 till source current is greater than zero .The moment it crosses zero and tries to increase in the negative direction ,the diode D_1 ceases conduction and the circuit transits to Mode 2 where in both the diodes are off(Fig. 2.4).

Now the capacitor 1 discharges and charges capacitor 2 slowly which was hitherto holding negative voltage across its terminals . The condition of both diodes off remain till a point when the voltage across capacitor 2 becomes equal to negative of

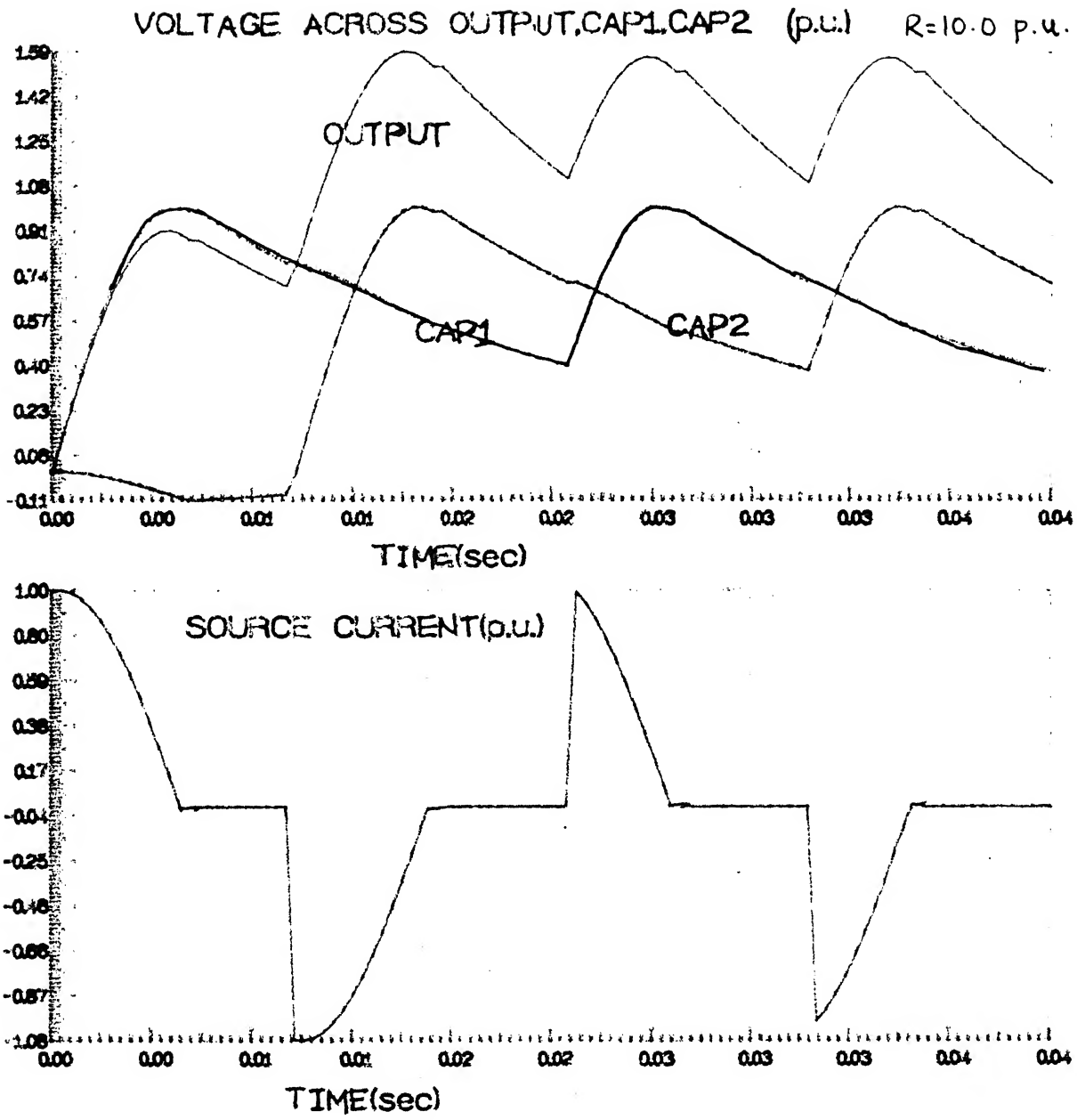


Fig.2.7 Loaded Transient Behaviour of the voltage doubling rectifier fed by ideal sine wave voltage source

the supply voltage . At this point D_2 turns on D_1 remains off (since voltage across it is greater than supply voltage) and the circuit transits to Mode 3 .The output voltage , capacitor 2 voltage increase and capacitor 1 voltage decreases.

Again the circuit transits to Mode 2 when the source current crosses zero . From here on the diodes D_1 and D_2 remain off till a point when voltage across capacitor 1 becomes less than supply voltage .

The circuit goes through above steps in transient and afterwards the voltage across capacitor 1 ,capacitor 2 and output follow a periodic pattern and the circuit moves in a cyclic order from Mode 1 to Mode 2 to Mode 3 to Mode 2 to Mode 1 and so on .

2.1.4.2 Average Output Voltage Vs. Load Resistance (p.u.) :

The characteristics is shown in Fig. 2.8 .Average output voltage rises as the load resistance increases . The output voltage reaches a value of approximately 2.0 p.u. at substantially high values of resistances. With the increased load resistances , the capacitors once charged to 1.0 p.u. do not discharge much in D_1 and D_2 off mode and as a result output average voltage goes up . It is seen from Fig. 2.8 that an acceptable voltage doubler with average output voltage greater than 1.9 p.u. must have a load resistance greater than approximately 100.0 p.u. Thus value of capacitance can be calculated for a given load and frequency.

2.1.4.3 Peak to Peak Output Voltage Ripple Vs. Load Resistance :

The characteristics is shown in Fig. 2.8 . The peak to peak voltage ripple reduces as we go on increasing the load resistance. The ripple reduces owing to the fact that capacitors do not lose their charge heavily as compared to the case when load resistance

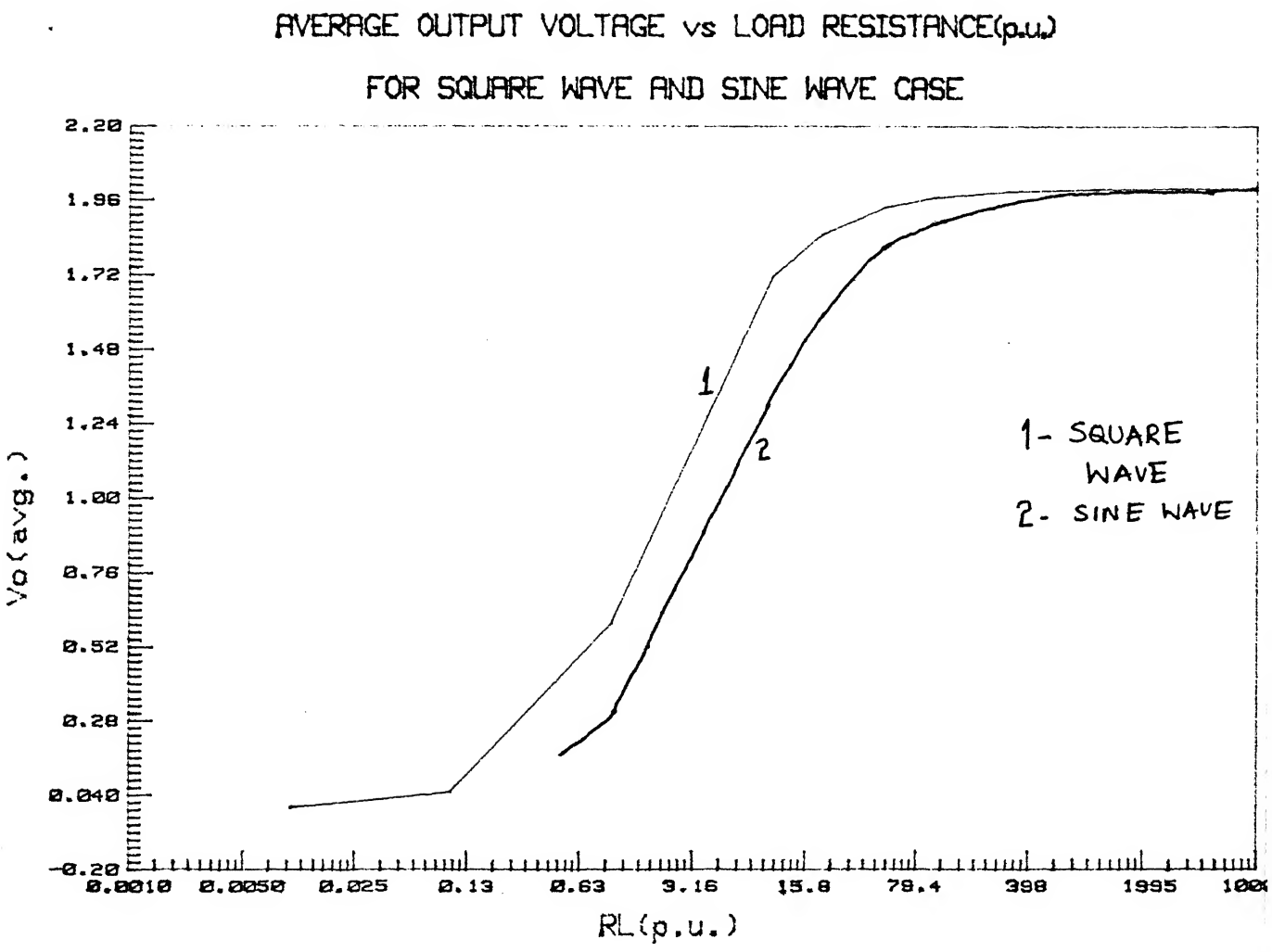


Fig.2.8 Average Output Voltage Vs Load Resistance characterstics for the voltage doubling rectifier fed by ideal sine wave voltage source

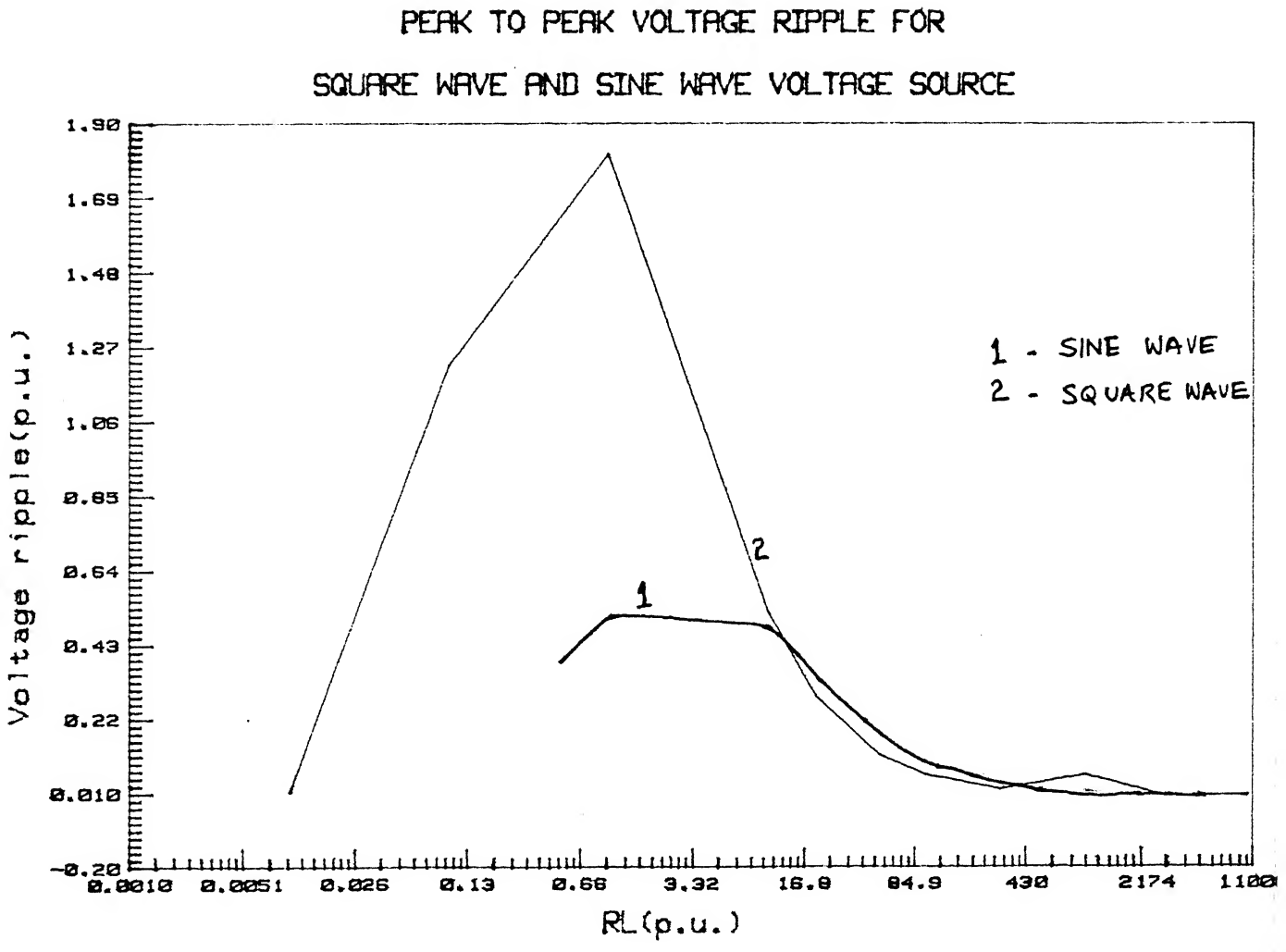


Fig.2.9 Peak to Peak output voltage Ripple Vs Load Resistance characterstics of the voltage doubling rectifier fed by ideal sine wave voltage source

15.8 p.u.

2.1.4.4 Average output current follows the same pattern as that of average output voltage for average output voltage is the product of average output current and load resistance .

2.1.4.5 When the load resistance is theoretically increased to infinity i.e. the output terminals of the power doubling rectifier are open circuited ,the following happens . Assuming we started with zero initial conditions ,in the first half cycle till $\omega t = \pi/2$,the capacitor 1 voltage will follow the input voltage and capacitor 2 voltage remains at zero voltage . At $\omega t = \pi/2$, the diode D_1 goes off and capacitor 1 remains at 1.0 p.u.for all values of time after it as there is no path to discharge . At $\omega t = \pi$, D_2 turns on voltage across capacitor 2 will be 180^0 out of phase with input voltage . At $\omega t = 3\pi/2$, D_2 goes off and capacitor 2 stays at 1.0 p.u. .The output voltage becomes 2.0 p.u. and remains at this value for any further values of time .

2.2 VOLTAGE DOUBLING RECTIFIER FED BY NON IDEAL SINE WAVE VOLTAGE SOURCE

The doubling rectifier (Fig. 2.10) fed by nonideal sine wave voltage source has three modes of operation . The non ideal sine wave voltage source has resistance , R_s and reactance, ωL_s . The modes are characterized by patterns of diode conduction . The modes of operation are

.. Mode 1 :D_1 ON , D_2 OFF, $\alpha < \omega t \leq \beta$

Mode 2 :D_1 OFF, D_2 OFF, $\beta < \omega t \leq \pi + \alpha$ and $\pi + \beta < \omega t \leq 2\pi + \alpha$

Mode 3 :D_1 OFF, D_2 ON , $\pi + \alpha < \omega t \leq \pi + \beta$

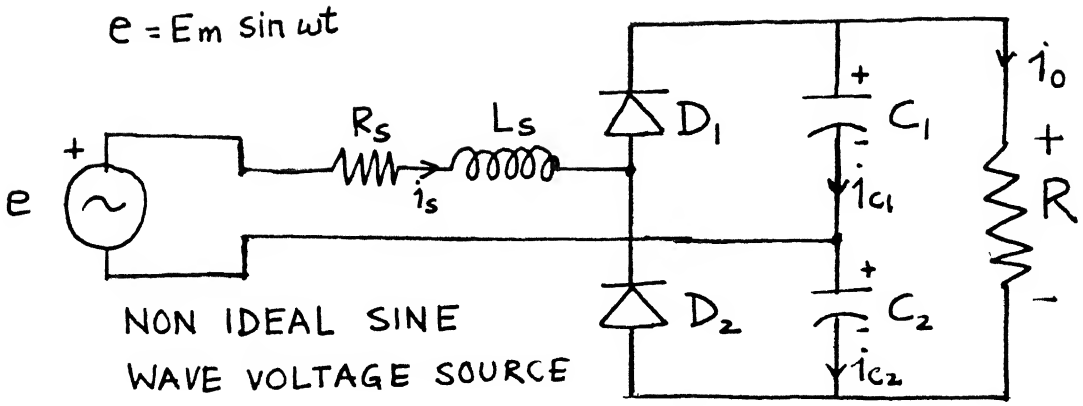


Fig.2.10 Voltage Doubling Rectifier fed by a non ideal sine wave voltage source.

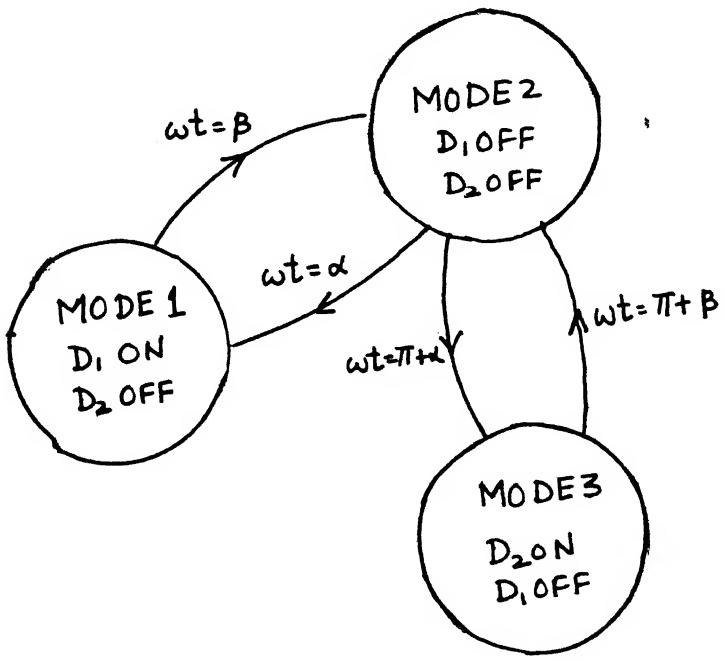


Fig.2.11 Mode Transition diagram for the circuit of Fig.2.10.

except for the fact that the voltage across capacitor 1 is not same as the suply voltage in mode 1 and voltage across capacitor 2 is not same as the negative of the supply voltage in mode 3. This is so because there is some voltage drop across source impendence.

2.2.1 DIFFERENTIAL EQUATIONS FOR MODES 1, 2 AND 3 AND THE METHOD OF SOLUTION

In this section the differential equations describing the rectifier in different modes have been written . The derivatives of voltage across capacitors 1 & 2 and source current have been used in simulating the behaviour of the doubling rectifier . The three variables of interest are V_{c1} , V_{c2} and i_s . The reference direction of capacitor voltage and current and source current are shown in the Fig. 2.10 . The equations have been normalised as per the normalisation scheme given in the beginning of the chapter . The diodes have been assumed to be ideal. The pattern of modes in steady state is 1 , 2 , 3 , 2 , 1 , 2 ... . The mode transition diagram is given in Fig. 2.11 .

Mode 1 (Fig. 2.12): In this mode D_1 is on and D_2 is off . Source current is positive . The circuit enters Mode 1 at $\omega t = \alpha$. The three differential equations are

$$E_m.\sin(\omega t) = i_s.R_s + L_s.d(i_s)/dt + V_{c1} \qquad [2.32]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c2})/dt \qquad [2.33]$$

$$\text{source current}, i_s = C.d(V_{c1})/dt + (V_{c1} + V_{c2})/R \qquad [2.34]$$

Normalising the above equations , we have

(from equation 2.32)

$$\sin(\omega t) = i_s.R_s/E_m + (L_s/E_m).[d(i_s)/dt] + V_{c1}/E_m$$

$$\sin(\omega t) = (i_s.R_s.\omega C)/(E_m.\omega C) + (L_s.\omega^2 C)/(E_m.\omega C).[d(i_s)/d(\omega t)]$$

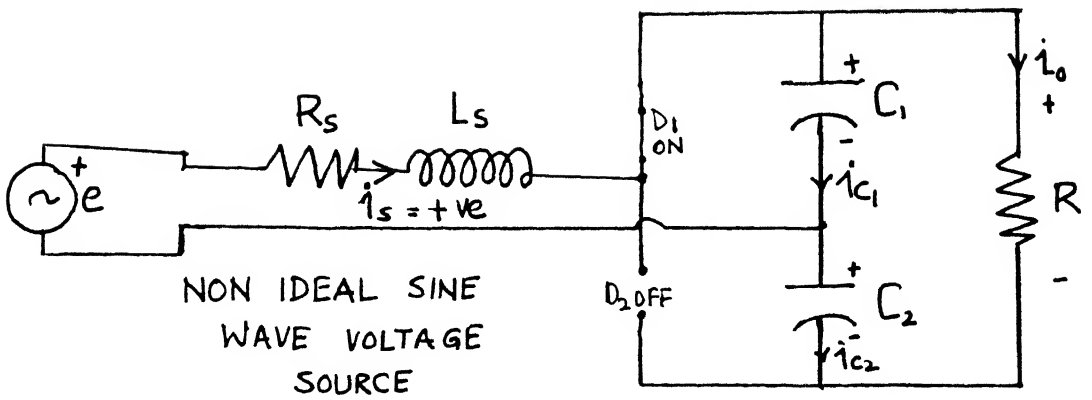


Fig.2.12 Equivalent circuit in Mode 1.

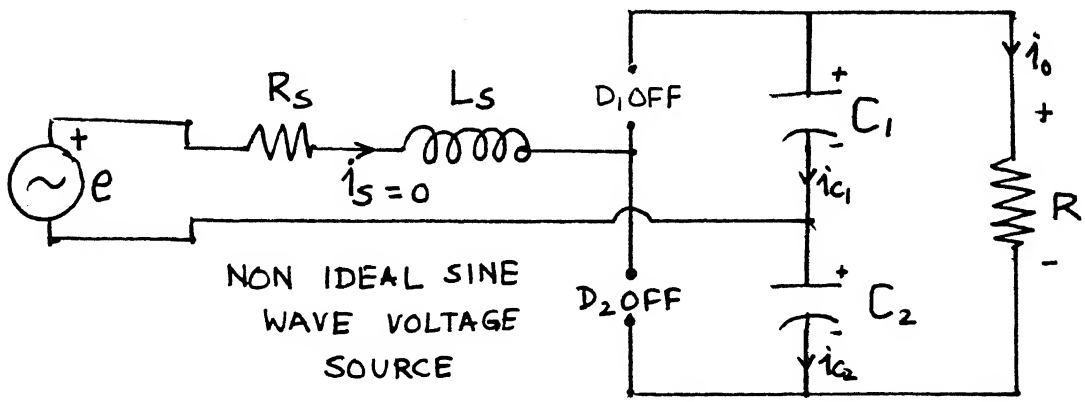


Fig.2.13 Equivalent circuit in Mode 2.

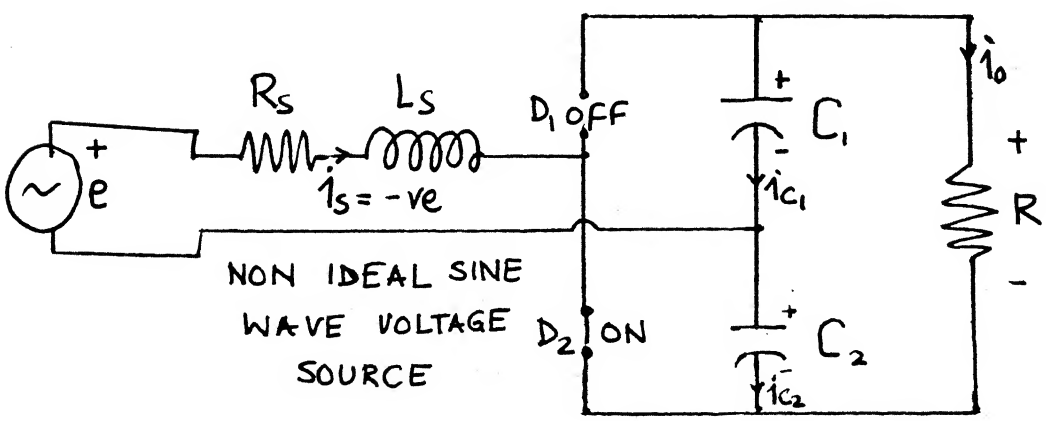


Fig.2.14 Equivalent circuit in Mode 3.

$$\sin(\omega t) = i_{sn}.R_{sn} + (\omega L_s)_n.\left[\frac{d(i_s)_n}{d(\omega t)}\right] + V_{c1n} \qquad [2.35]$$

(from equation 2.33)

$$(V_{c1} + V_{c2})/E_m = - (RC/E_m).d(V_{c2})/dt$$

$$V_{c1n} + V_{c2n} = - (RC.\omega)/(E_m).d(V_{c2})/d(\omega t)$$

$$V_{c1n} + V_{c2n} = - R_n.\left[\frac{dV_{c2n}}{d(\omega t)}\right] \qquad [2.36]$$

(from equation 2.34)

$$i_s/(E_m.\omega C) = C/(E_m.\omega C).d(V_{c1})/dt + (V_{c1} + V_{c2})/(R.E_m.\omega C)$$

$$i_{sn} = \left[\frac{d(V_{c1})_n}{d(\omega t)}\right] + \frac{(V_{c1n} + V_{c2n})}{R_n} \qquad [2.37]$$

In all the equations derived above suffix n represents normalised variables e.g. $(\omega L_s)_n = \omega^2.L_s.C$ represents normalised source reactance .

Equations 2.32 , 2.33 , 2.34 , 2.35 , 2.36 and 2.37 describe the operation of voltage doubling rectifier in Mode 1 .

MODE 2 (Fig. 2.13) : In this mode both the diodes D_1 and D_2 are off . The circuit is characterised by source current , $i_s = 0$ .The circuit enters mode 2 at $\omega t = \beta$ when source current becomes zero . The three differential equations are

$$\text{source current }, i_s = 0 \qquad [2.38]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c2})/dt \qquad [2.39]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c1})/dt \qquad [2.40]$$

Normalised equations can be written as follows

$$i_{sn} = 0 \qquad [2.41]$$

Equations 2.39 and 2.40 are of the kind of equation 2.33 , hence the normalised equations directly become

$$V_{c1n} + V_{c2n} = - R_n.\left[\frac{dV_{c1n}}{d(\omega t)}\right] \qquad [2.42]$$

$$V_{c1n} + V_{c2n} = - R_n . \left[\frac{dV_{c2n}}{d(\omega t)} \right] \qquad [2.43]$$

Equations 2.38 , 2.39 , 2.40 , 2.41 , 2.42 and 2.43 describe the operation of the doubling rectifier in mode 2 .

MODE 3 (Fig. 2.14) : In this mode diode D_1 is off and diode D_2 is off . The circuit enters mode 3 at $\omega t = \pi + \alpha$ when negative of the supply voltage becomes greater than voltage across capacitor 2 . The source current is negative . The three differential equations of the circuit are derived below

$$E_m . \sin(\omega t) = i_s . R_s + L_s . d(i_s)/dt - V_{c2} \qquad [2.44]$$

$$(V_{c1} + V_{c2}) / R = - C . d(V_{c1})/dt \qquad [2.45]$$

$$\text{source current}, i_s = - C . d(V_{c2})/dt - (V_{c1} + V_{c2})/R \qquad [2.46]$$

Normalisation of the equations can be done as earlier and the resulting equations in per unit are given below

$$\sin(\omega t) = i_{sn} . R_{sn} + (\omega L_s)_n . \left[\frac{d(i_s)_n}{d(\omega t)} \right] - V_{c2n} \qquad [2.47]$$

$$V_{c1n} + V_{c2n} = - R_n . \left[\frac{dV_{c1n}}{d(\omega t)} \right] \qquad [2.48]$$

$$i_{sn} = \left[\frac{d(V_{c1})_n}{d(\omega t)} \right] + \frac{(V_{c1n} + V_{c2n})}{R_n} \qquad [2.49]$$

Equations 2.44 , 2.45 , 2.46 , 2.47 , 2.48 and 2.49 describe the operation of the doubling rectifier in mode 3 .

METHOD OF SOLUTION : The equations derived above for the operation of the doubling rectifier in different modes have been programmed on HP-UX 9000 in Fortran 77 . The expressions for the first derivatives of the variables V_{c1} , V_{c2} and i_s are required . The three simultaneous equations in variables V_{c1} , V_{c2} and i_s are

Appendix 3 gives the details of this subroutine.

In mode 1 the computed values of the source current are continuously monitored and as soon as the zero crossing of source current is detected , the program flow is either transferred to computations in Mode 2 or Mode 3 . Normally the program flow is transferred to computations in Mode 2 .

In mode 2 the computed values of the variables V_{c1} and V_{c2} are continuosly monitored .The program flow is either transferred to Mode 1 or Mode 3 depending on whether the supply voltage is greater than voltage across capacitor 1 or the negative of the supply voltage is greater than voltage across capacitor 2 .

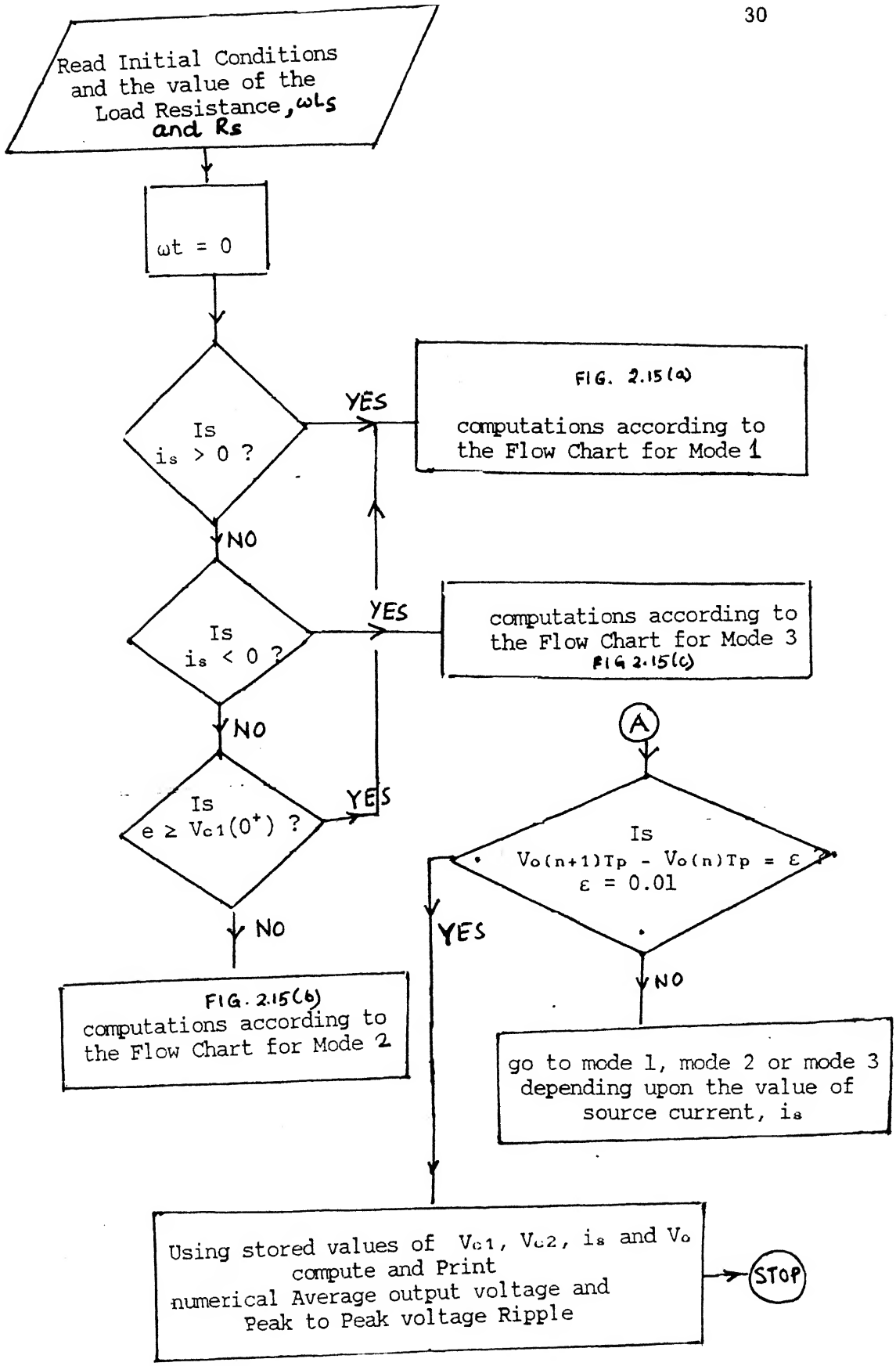
In mode 3 the computed values of the source current are continuously monitored and as soon as the zero crossing of source current is detected , the program flow is either transferred to computations in Mode 2 or Mode 3 . Normally the program flow is transferred to computations in Mode 2 .

The conditions which decide these transfers are already described in the beginning of this chapter .Flow chart of Fig.2.15 further describes this scheme .The computed values of the variables V_{c1} , V_{c2} and i_s are stored appropriately to be used later for computation of average output voltage and peak to peak output voltage ripple .

2.2.2 METHOD OF COMPUTATION OF AVERAGE OUTPUT VOLTAGE AND PEAK TO PEAK OUTPUT VOLTAGE RIPPLE

This is computed in the manner as follows :

The data points are available every 'tstep' radians . 'tstep' is the step size in computation . We assume the output voltage to remain constant over 'tstep' radians .The smaller the value of 'tstep' ,higher will be the computational accuracy . Hence the



1.2.15 **Flow chart for the Simulation of the Voltage doubling rectifier fed by non ideal sine wave source**

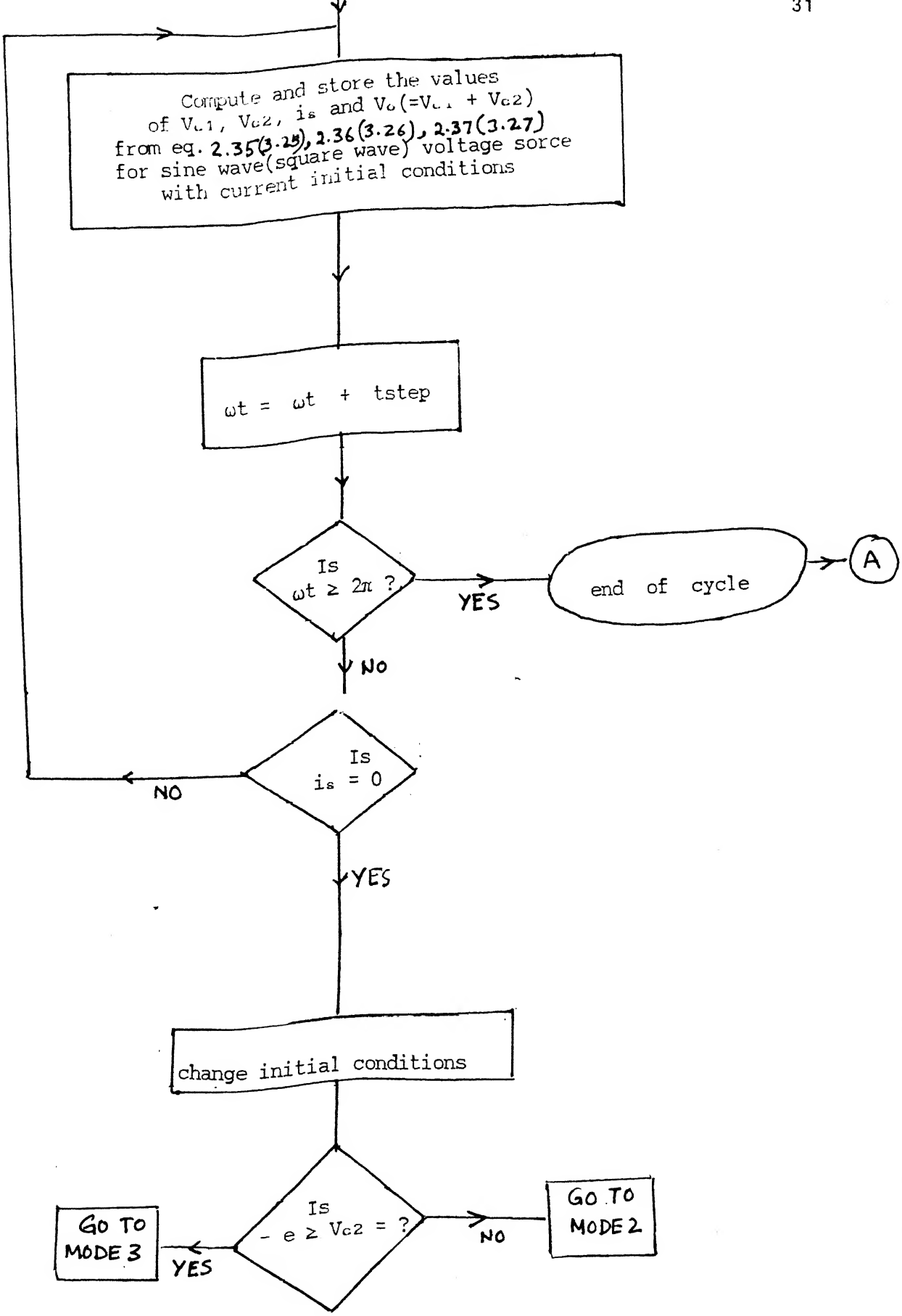

Compute and store the values of Vc1, Vc2, is and Vo(=Vc1 + Vc2) from eq. 2.35(3.25), 2.36(3.26), 2.37(3.27) for sine wave(square wave) voltage sorce with current initial conditions
ωt = ωt + tstep
Is ωt ≥ 2π ?
YES
end of cycle
A
NO
Is is = 0
NO
YES
change initial conditions
Is - e ≥ Vc2 = ?
NO
GO TO MODE 2
GO TO MODE 3
YES

FIG. 2.15 (a)

FLOW CHART FOR MODE 2

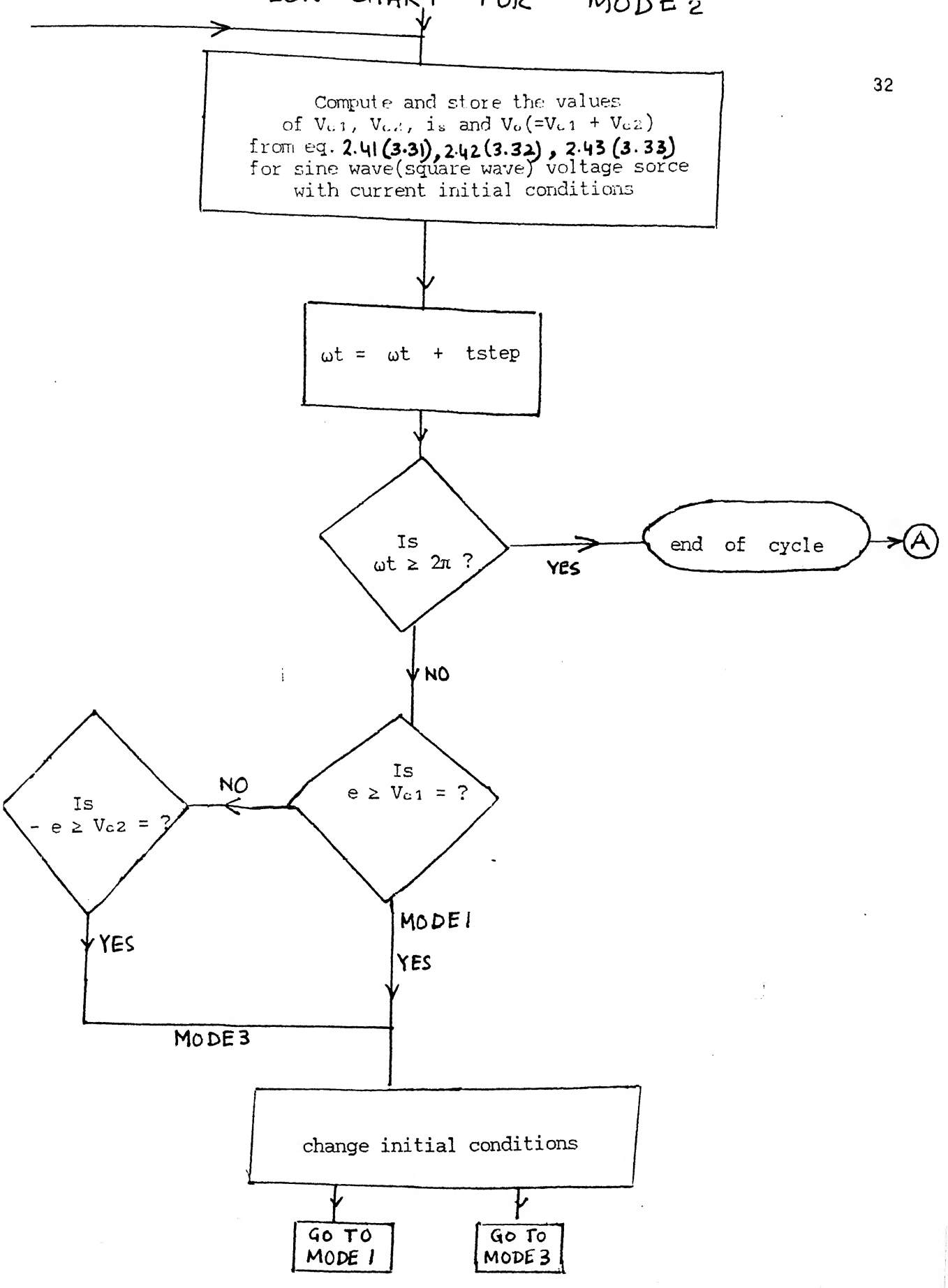
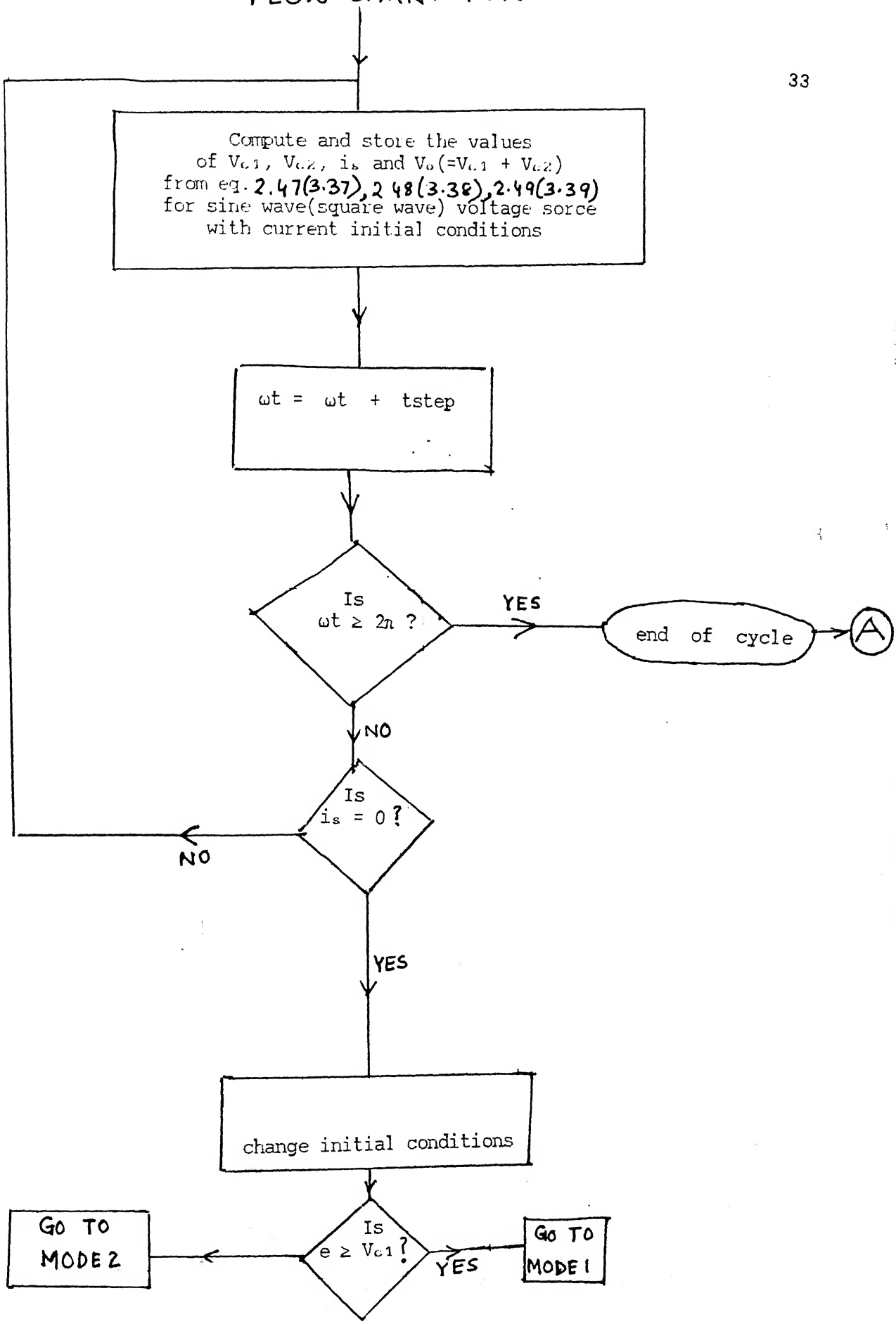


FIG. 2.15(b)

FLOW CHART FOR MODE 3



average output voltage in per unit is

$$V_{oavgn} = \sum_{i=1}^{k} \frac{(V_{c1ni} + V_{c2ni})}{k}$$

where k = no. of data points over a period of 2π radians. In the complete process of transient and steady state there can be p.k data points where p is the no. of cycles taken by the circuit in reaching the steady state. Only last k datapoints, however, are retained for these are the data points corresponding to the steady state of the circuit. The data points during the transient state are only needed for plotting .

The maximum and minimum values of the output voltage are picked and the difference is outputed as peak to peak output voltage ripple .

2.2.3 DISCUSSION OF THE SIMULATION RESULTS

In this section the general behaviour of the doubling rectifier has been studied . The transient behaviour,steady state behaviour,average output voltage and peak to peak voltage ripple for different values of load resistances and source reactances have been calculated and shown in Figs.2.16, 2.17 and 2.18.

These results are discussed below :

2.2.3.1 Loaded transient and steady state behaviour of the doubling rectifier

The behaviour is shown in Fig. 2.16 . The doubling rectifier with load resistance of 10.0 p.u. , source resistance of 0.01 p.u. and source inductive reactance of 0.05 p.u. was simulated for studying its transient and steady state behaviour .

Fig. 2.16 shows the simulated output voltage , voltage

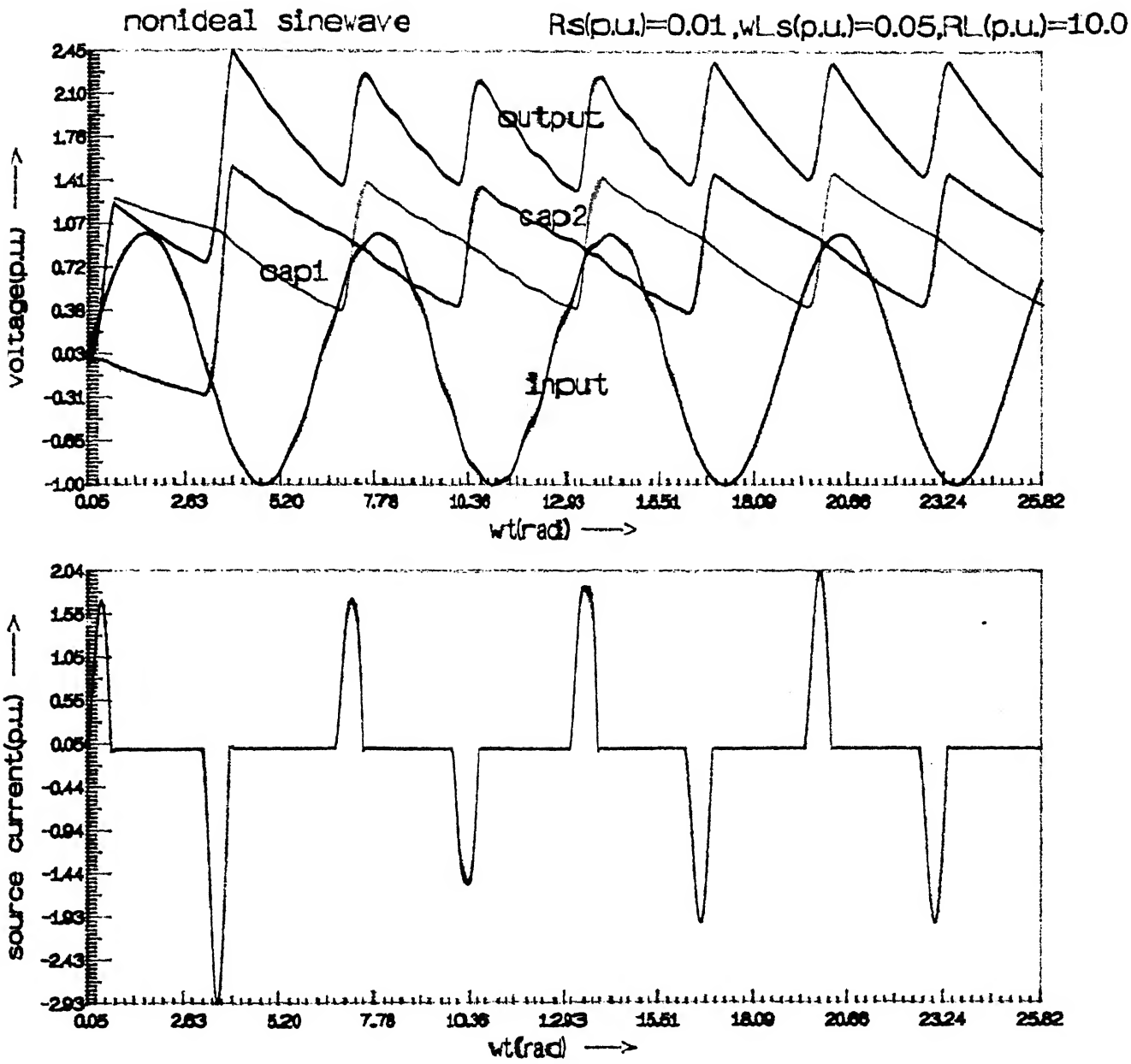


Fig.2.16 Loaded Transient Behaviour for the voltage doubling rectifier fed by non ideal sine wave voltage source

and input voltage .The doubling rectifier is excited from cold and its transient behaviour is recorded .At $\omega t = 0^+$,diode D_1 turns on as the supply voltage is larger than the voltage across capacitor 1 (being zero). Source current, i_s jumps to a value decided by the series combination of R-L-C. Source current is a sinusoidal pulse. The diode D_2 is off as it is reverse biased. The voltage across capacitor 2 increases in the negative direction. The circuit remains in Mode 1 till source current is greater than zero .The moment it crosses zero and tries to increase in the negative direction, the diode D_1 ceases conduction and the circuit transits to Mode 2 where in both the diodes are off.

Now the capacitor 1 discharges and charges capacitor 2 slowly which was hitherto holding negative voltage across its terminals. The condition of both diodes off remain till a point when the voltage across capacitor 2 becomes equal to negative of the supply voltage. At this point D_2 turns on D_1 remains off (since voltage across it is greater than supply voltage) and the circuit transits to Mode 3. The output voltage, capacitor 2 voltage increase and capacitor 1 voltage decreases.

Again the circuit transits to Mode 2 when the source current becomes zero. From here on the diodes D_1 and D_2 remain off till a point when voltage across capacitor 1 becomes less than supply voltage .

The circuit goes through above steps in transient and afterwards the voltage across capacitor 1 ,capacitor 2 and output follow a periodic pattern and the circuit moves in a cyclic order from Mode 1 to Mode 2 to Mode 3 to Mode 2 to Mode 1 and so on. The mode transition diagram is shown in Fig.2.11.

2.2.3.4 *PERIODICITY OF THE OUTPUT VOLTAGE WAVEFORM*

The simulation results were recorded for various of load resistances and a very peculiar behaviour of the doubling rectifier was noticed.

Normally the output voltage has a ripple frequency twice as that of the input supply frequency. But, when the doubling rectifier is fed by a nonideal sinusoidal voltage source, the output voltage has a ripple frequency twice as that of the input supply voltage frequency till a critical value of the load resistance. The critical value is 30.61 p.u. when the source reactance is 0.05 p.u., source resistance is 0.01 p.u. and load being supplied is 10.0 p.u. The frequency of the output voltage keeps on reducing as the value of load resistance is increased beyond 30.61 p.u. At very large values of load resistances the ripple frequency is so low that for all practical purposes the output voltage can be assumed to be flat. The table 2.1 shows the growth in the time period of the ripple in the output voltage.

2.2.3.2 VARIATION OF THE AVERAGE OUTPUT VOLTAGE WITH LOAD RESISTANCE AND SOURCE REACTANCE

Average output voltage vs. source reactance :

The characteristics is shown in Fig. 2.17. From Fig. it is clear that the average output voltage falls both at very low values of ωL_s and at at relatively large values of ωL_s. The average output voltage is close to the ideal value of 2.0 p.u. for the range of ωL_s = 0.015 to 0.07.

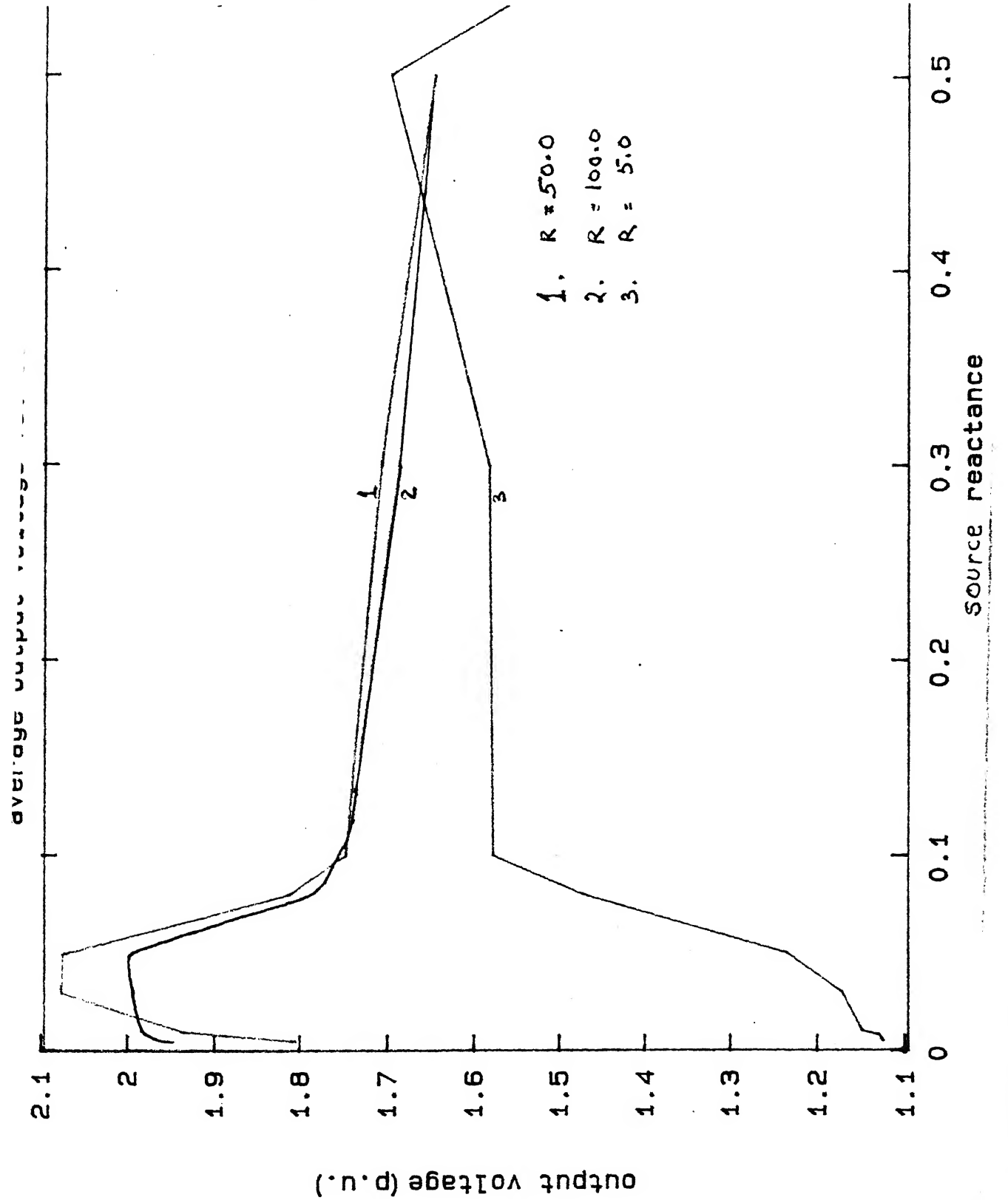
From the wave forms of the Fig.2.16, the source current is seen to have sharp sinusoidal pulses at ωL_s = 0.05 p.u. As ωL_s reduces towards ideal value of zero, the amplitude of the pulses become very large as analysed in section in 2.1. Due to these sharp pulses of source current, the diodes D_1 and D_2 turn off after conducting for very short intervals of time in positive and

TABLE 2.1

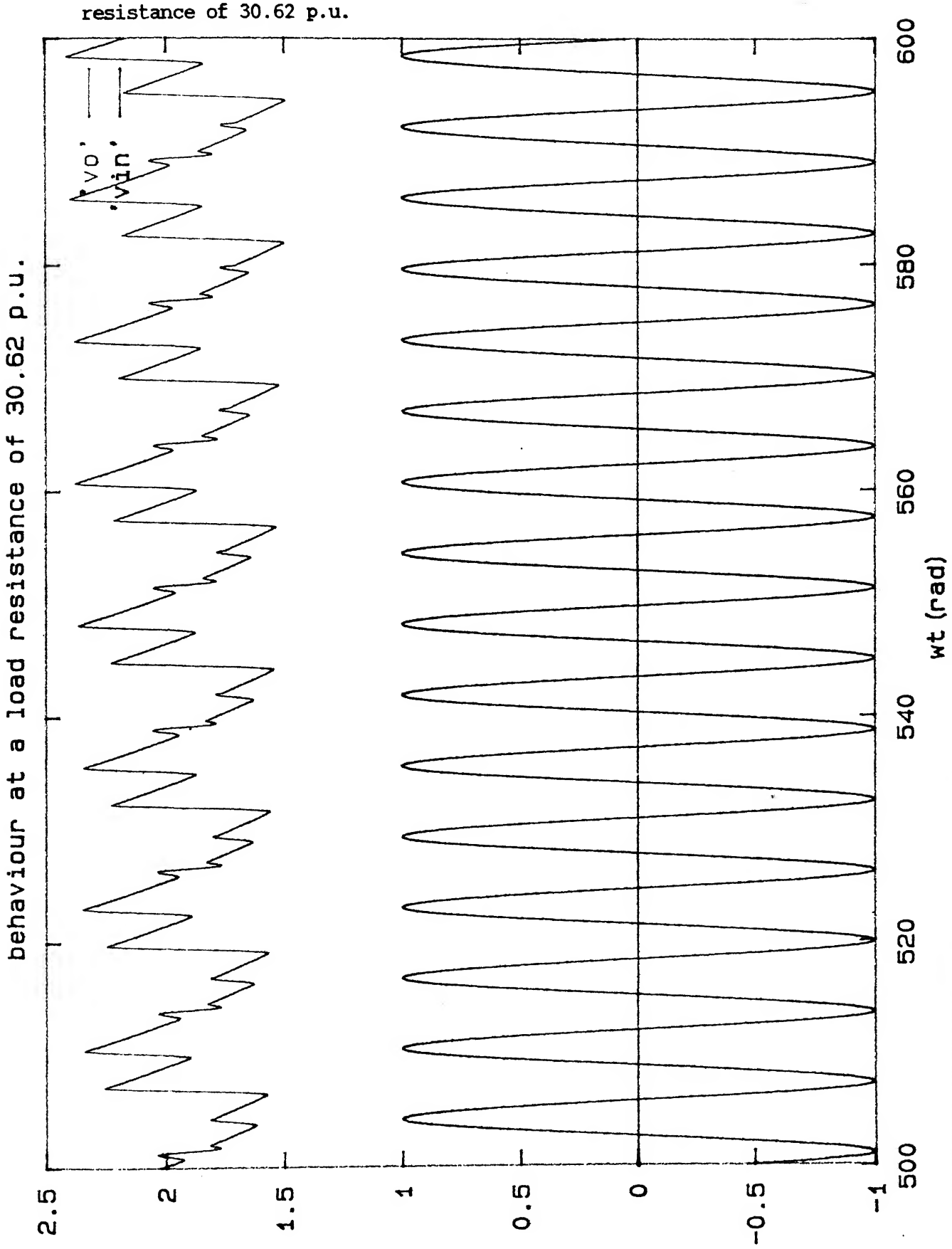
VARIATION OF RIPPLE FREQUENCY OF THE OUTPUT VOLTAGE WITH VARIATION IN LOAD RESISTANCE

	Load Resistance (p.u.)	Time period as a multiple of of input supply time period
1.	10.0	0.5
2.	25.0	0.5
3.	30.61	0.5
4.	30.62	1.0
5.	39.32	2.0
6.	39.33	4.0
7.	100.51	11.0
8.	100.52	26.0
9.	1000.0	very large(see fig.2.20)

Fig.2.17 "Average Output Voltage Vs Source Reactance for varying Load Resistances characterstics" for the voltage doubling rectifier fed by non ideal sine wave voltage source



2.19 Loaded Transient behaviour for the voltage doubling rectifier fed by nonideal sine wave voltage at a load resistance of 30.62 p.u.



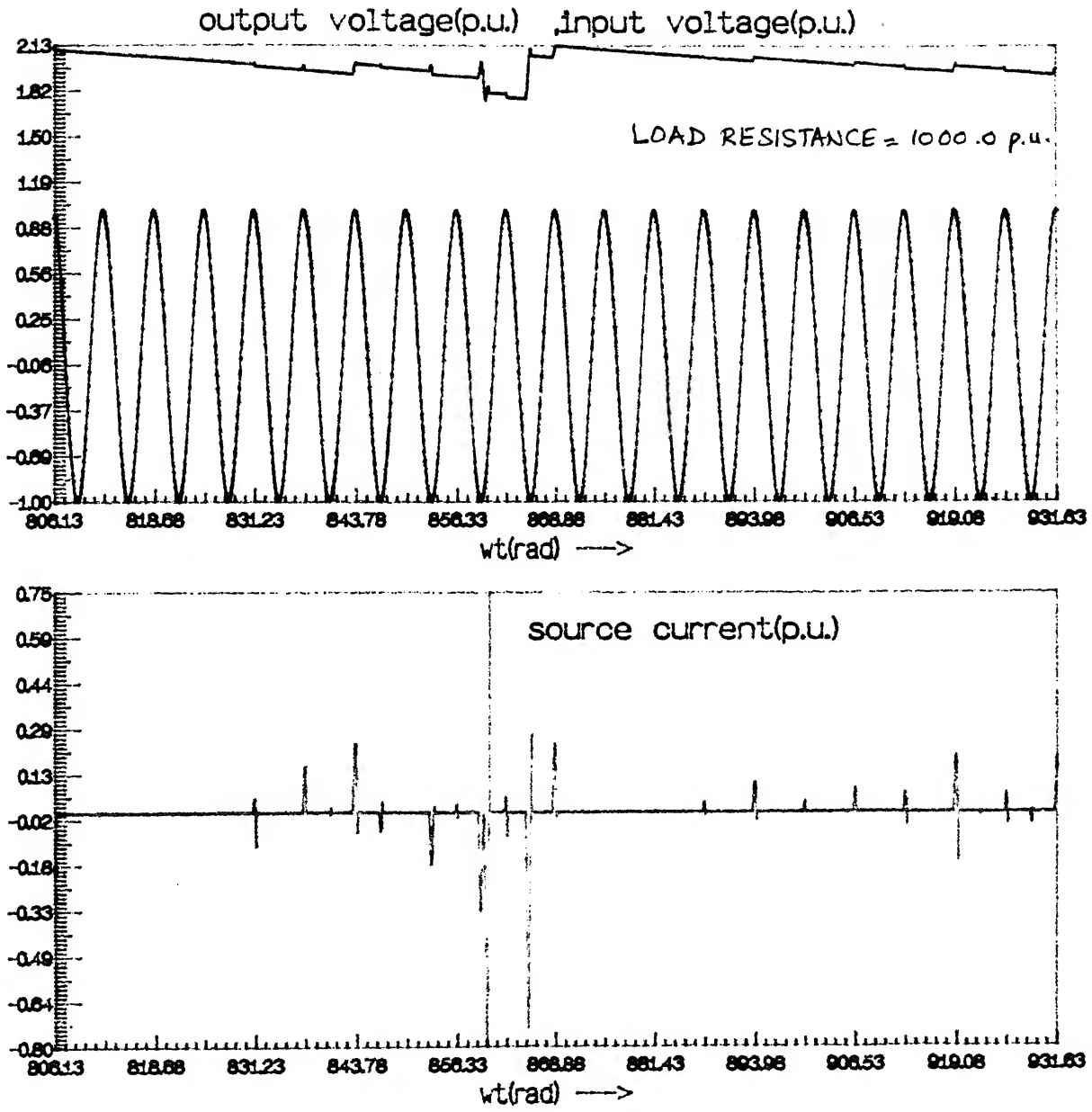


Fig.2.20 Loaded Transient behaviour for the voltage doubling rectifier fed by non ideal sine wave voltage source at a load resistance of 1000.0 p.u.

negative half cycles respectively.Therefore the capacitors supply energy to the load for most part of the cycle and thus output voltage falls for most part of the cycle. The average output voltage, hence, is low at low values of ωL_s.

At high values of ωL_s (> 0.07 p.u.) the peak source current reduces and due to large values of the source reactance the conduction period of the diodes in the positive and negative half cycles increases. However, the average output voltage falls as the inductive circuit is not able to transfer charge quickly.

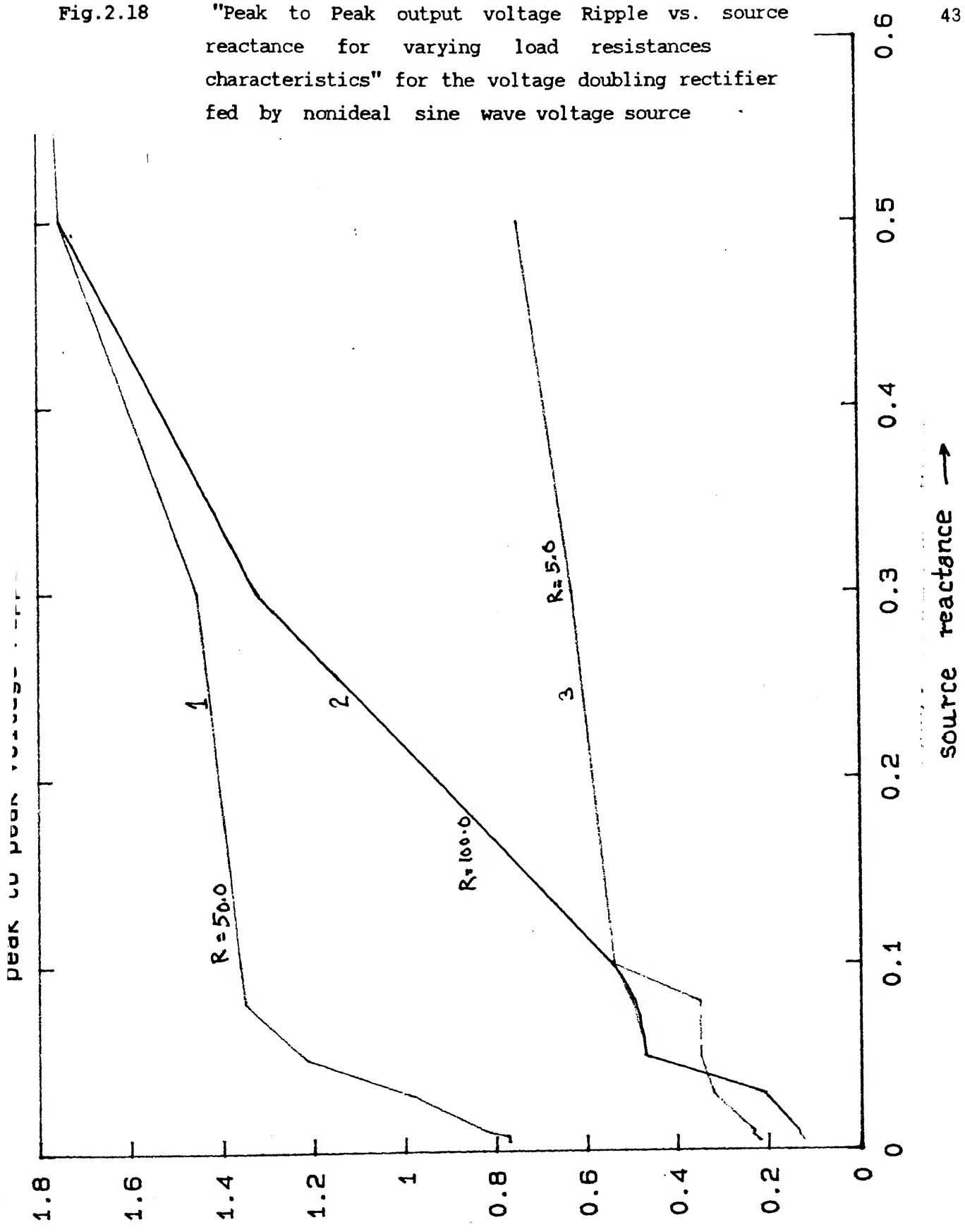
Average output voltage vs. load resistance :

The behaviour of the output average voltage vs. load resistance is quite complex in nature.The average output voltage rises as the load resistance is increased for the values of ωL_s in the range

from 0.015 to 0.07. At higher values of the source reactances (>0.07 p.u.), the average output voltage rises till a critical value of the load resistance. Increase in the load resistances beyond this value causes a decrease in the average output voltage. For small values of the source reactance, as the load resistance is increased, the capacitors once charged do not lose much of their stored energy and as a result the output voltage rises. However, at large values of the source reactances (>0.07 p.u.), the increase in the load resistance causes a decrease in the average output voltage because the energy is trapped in the source inductance.

2.2.3.3 VARIATION OF PEAK TO PEAK OUTPUT VOLTAGE RIPPLE WITH LOAD RESISTANCE AND SOURCE REACTANCE

Fig.2.18 "Peak to Peak output voltage Ripple vs. source reactance for varying load resistances characteristics" for the voltage doubling rectifier fed by nonideal sine wave voltage source



The characteristics is shown in Fig. 2.18. As explained in sec.2.2.3.2 above, the ripple voltage increases as the source reactance is increased. At low values of the ωL_s, the diodes conduct large current pulses for shorter durations. These large current pulses cause sharp voltage rises across capacitors 1 & 2. For most part of the cycle diodes are off and capacitors discharge from their peak levels causing a large peak to peak output voltage ripple.

At large values of source reactances, the conduction period of the diodes increase and due to the continuous change in the supply voltage (the input sinusoidal voltage magnitude is continuously changing) the ripple in output voltage increases. The behaviour of the percentage ripple is complex due to changes in the average output voltage with source reactance(fig. 2.17).

Peak to Peak output voltage ripple vs. load resistance:

The behaviour of the peak to peak output voltage ripple is inverse of the behaviour of the average output voltage. as seen in fig. 2.18.

CHAPTER 3

VOLTAGE DOUBLING RECTIFIER FED BY SQUARE WAVE VOLTAGE SOURCE

In this chapter analysis and simulation of the voltage doubling rectifier fed by ideal and non ideal square wave voltage source has been done. Simulation results have been discussed. Some important conclusions have been made.

3.1 VOLTAGE DOUBLING RECTIFIER FED BY AN IDEAL SQUARE WAVE VOLTAGE SOURCE

The doubling rectifier of Fig.3.1 with ideal square wave voltage source has two modes of operation . These modes are characterised by the patterns of diode conduction . The mode transitions are shown in Fig. 3.2 .The modes are :

Mode 1 : D_1 on , D_2 off, $0 < \omega t < \pi$.

Mode 2 : D_1 off , D_2 on , $\pi < \omega t < 2\pi$.

The description of each mode is as follows :

MODE 1 : The equivalent circuit for this mode is shown in Fig.3.3. In this mode the diode D_1 starts conduction at $\omega t = 0$ as the supply voltage is larger than capacitor 1 voltage . At $\omega t = 0$,an impulse of current flows through diode D_1 as the voltage across capacitor 1 is less than E_m .Voltage across capacitor now jumps to

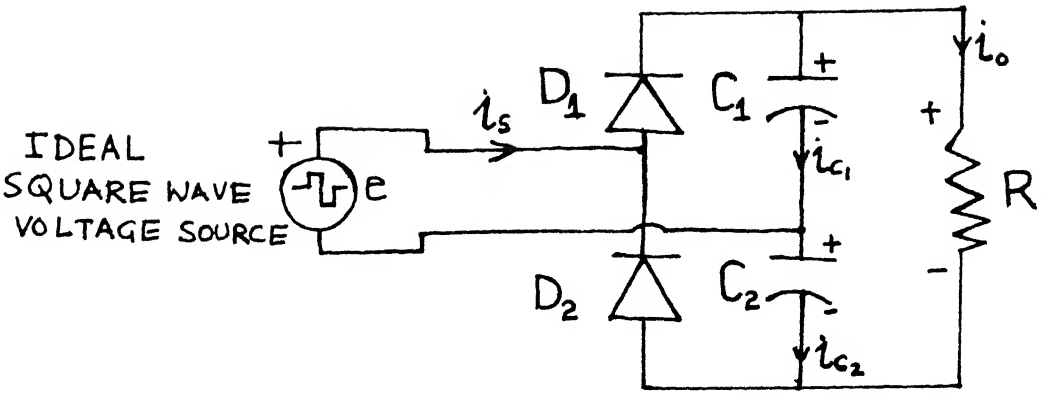


Fig.3.1(a) Voltage Doubling Rectifier fed by ideal square wave voltage source.

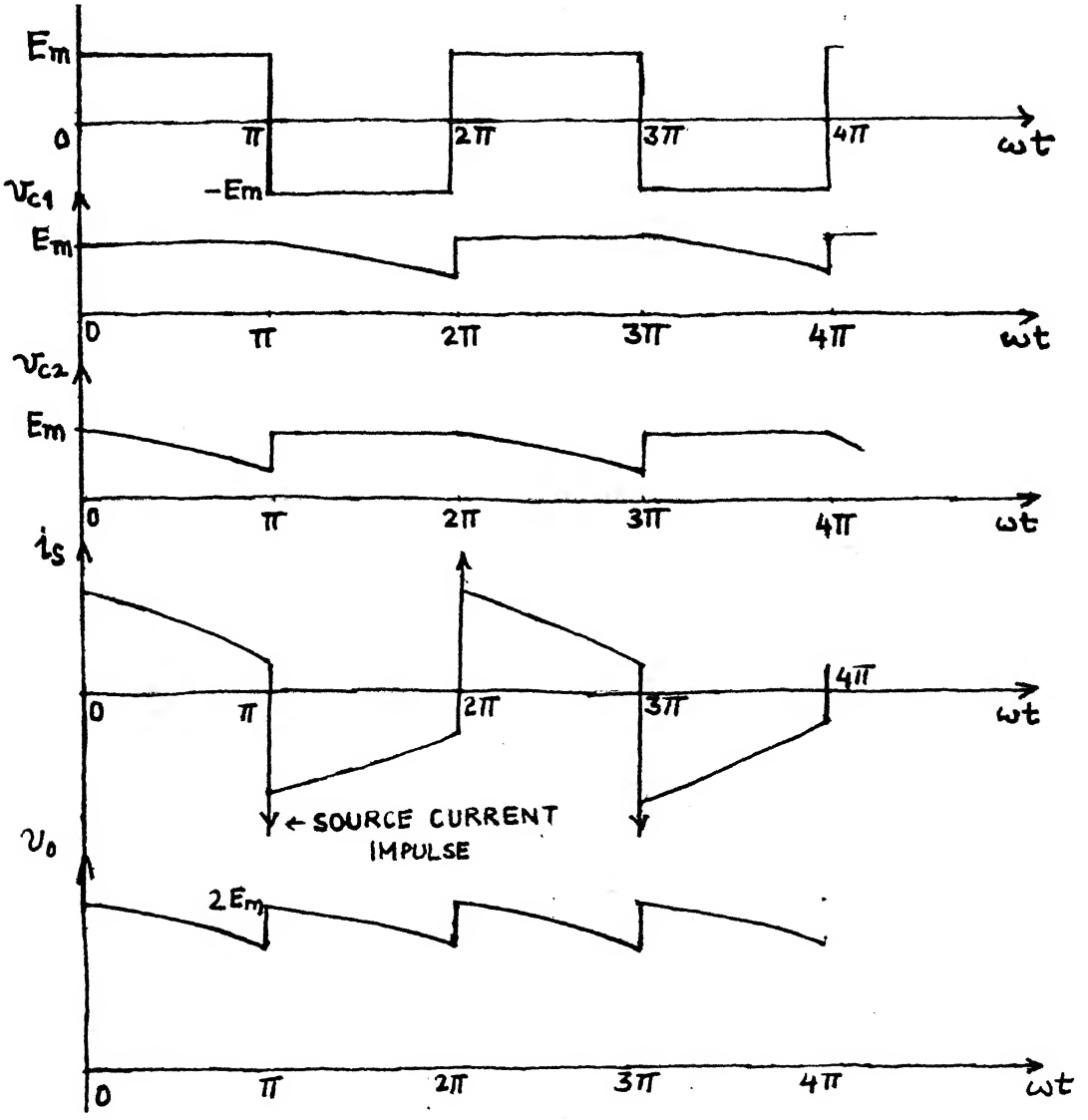


Fig.3.1(b) Typical circuit waveforms.

E_m from a value less than E_m as a result of this impulse of current .Had there not been any parallel path across capacitor 1, diode D_1 would have stopped conduction for the source current would then have become zero .Since we have a series R-C in parallel with capacitor 1 , the diode D_1 keeps on conducting to supply charge to capacitor 2 and hence the source current (same as diode D_1 current) is not zero .Voltage across capacitor C_2 decreases in Mode 1 . At $\omega t = \pi$, the supply voltage jumps to $-E_m$ and the circuit transits to Mode 2 due to the following :
At $\omega t = \pi^-$,the diode D_1 is on and diode D_2 is off . At $\omega t = \pi$, the source voltage jumps to $-E_m$ .The voltage across diode D_1 reverses and becomes $-2E_m$ .This causes the source current to reverse and as a result turn diode D_1 off . Diode D_2 is forward biased as the negative of the supply voltage is larger than the voltage across capacitor 2 . This turns diode D_2 on .

MODE 2 : The equivalent circuit for this mode is shown in Fig.3.4. At $\omega t = \pi^+$, the diode D_2 turns on as the negative of the supply voltage is larger than the voltage across capacitor 2 . Source experiences a negative impulse of current at $\omega t = \pi^+$. This is due the difference(ΔV) in voltage across capacitor 2 and negative of supply voltage at $\omega t = \pi^+$.The strength of the impulse is ($C.\Delta V$). Larger the difference larger will be the strength of the impulse. The diode D_2 remains on till $\omega t = 2\pi$ when D_1 turns on owing to the reasons explained above in Mode 1 .The circuit transits to Mode 1 at $\omega t = 2\pi$ .Cyclic change in modes of operation is shown in Fig. 3.2 . The patterns of modes in steady state is

1, 2, 1, 2.. . The typical waveforms of V_{c1}, V_{c2} and i_s are given in Fig. 3.1(b) .

3.1.1 DIFFERENTIAL EQUATIONS OF THE DOUBLING RECTIFIER FOR MODES 1 AND 2 AND THE METHOD OF SOLUTION

In this section the differential equations describing the rectifier in different modes have been derived . The equations are solved for the expressions of V_{c1} and V_{c2} . The two variables of interest are V_{c1} and V_{c2} in this circuit . The reference directions for capacitor voltages and currents are shown in Fig.3.1 . KVL and KCL have been applied to derive differential equations . The diodes D_1 and D_2 have ben assumed to be ideal .

Normalisation Scheme : Normalisation scheme is same as that given in chapter 2 (Sec 2.1.1) .The equations have been converted in p.u. form using this normalisation scheme .All normalised variables have been shown with subscripts n .

MODE 1 (Fig. 3.3) : In this mode D_1 is on and D_2 is off . Source current is positive . The three differential equations in Mode 1 are given below.The circuit enters Mode 1 at $\omega t = 0^+$.

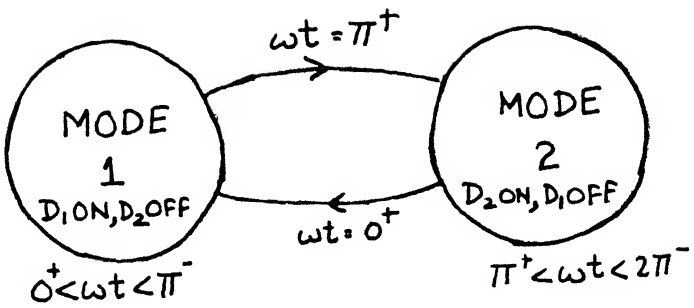


Fig.3.2 Mode Transition Diagram for the voltage doubling rectifier fed by an ideal square wave voltage source

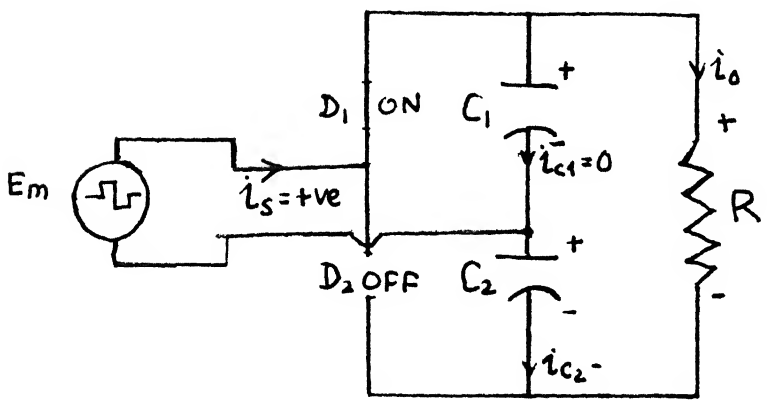


Fig.3.3 Equivalent Circuit in Mode 1.

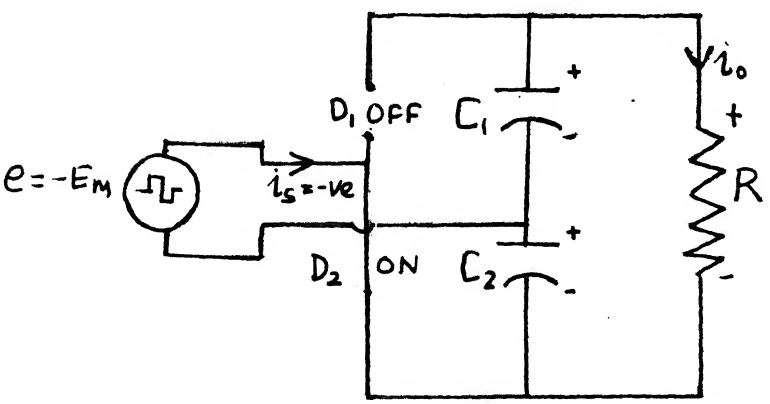


Fig.3.4 Equivalent Circuit in Mode 2.

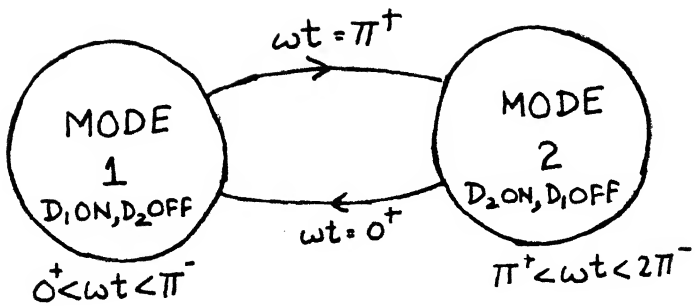


Fig.3.2 Mode Transition Diagram for the voltage doubling rectifier fed by an ideal square wave voltage source

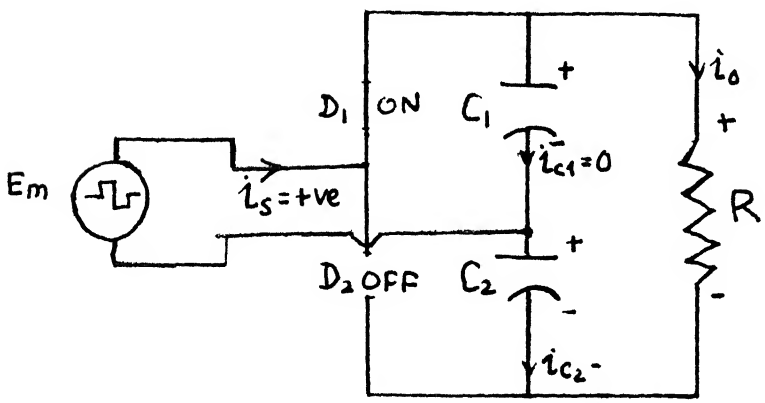


Fig.3.3 Equivalent Circuit in Mode 1.

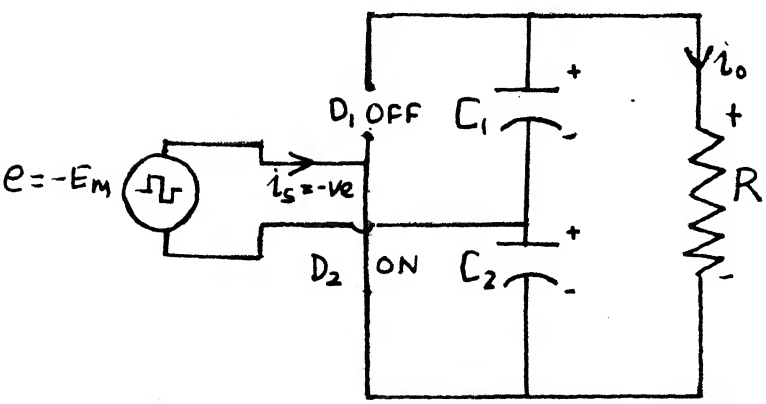


Fig.3.4 Equivalent Circuit in Mode 2.

$$V_{c1} = E_m \qquad [3.1]$$

$$(V_{c1} + V_{c2})/R = -C.d(V_{c2})/dt \qquad [3.2]$$

$$\text{Source current }, i_s = (V_{c1} + V_{c2})/R \qquad [3.3]$$

[3.1] and [3.2] give

$$(1/RC + D)V_{c2} = -E_m/RC \quad ; \text{ where } D \equiv d/dt$$

Solution of above differential equation gives

$$V_{c2} = -E_m + [(V_{c2}(0^+) + E_m].\exp(-\omega t/\omega.RC) \qquad [3.4]$$

where $V_{c2}(0^+)$ is the voltage across capacitor 2 at $\omega t = 0^+$. Normalised equations as per normalisation scheme discussed above for V_{c1} ,V_{c2} and i_s are given below :

$$V_{c1n} = 1.0 \qquad [3.5]$$

$$V_{c2n} = -1 + [V_{c2n}(0^+) + 1].\exp(-\omega t/R_n) \qquad [3.6]$$

where $R_n = \omega RC$ (normalised load resistance)

$$i_{sn} = (V_{c1n} + V_{c2n})/R_n \qquad [3.7]$$

In steady state the value of $V_{c2}(0^+)$ is E_m . Hence equation 3.6 changes to the following

$$V_{c2n} = -1 + 2.\exp(-\omega t/R_n) \qquad [3.8]$$

Equations 3.1 , 3.4 , 3.5 and 3.6 describe the operation of voltage doubling rectifier in Mode 1 .

MODE 2 (Fig. 3.4) : This mode is characterised by the condition that diodes D_1 is off and D_2 is on . In other words source current ,i_s is negative .This mode starts at $\omega t = \pi^+$ .The three

differential equations under this condition are given below :

$$V_{c2} = E_m \qquad [3.9]$$

$$(V_{c1} + V_{c2})/R = -C.d(V_{c1})/dt \qquad [3.10]$$

$$i_s = -(V_{c1} + V_{c2})/R \qquad [3.11]$$

Equations 3.9 and 3.10 give

$$(D + 1/RC)V_{c1} = - E_m/RC \quad ; \text{ where } D \equiv d/dt$$

Applying initial condititons that $V_{c1} = V_{c1}(\pi)$ at $\omega t = \pi^+$ and solving ,we have

$$V_{c1} = -E_m + [E_m + V_{c1}(\pi^+)].\exp \{-(\omega t-\pi)/\omega RC\} \qquad [3.12]$$

In steady state $V_{c1}(\pi^+) = E_m$ .Hence equation 3.12 modifies to

$$V_{c1} = -E_m + 2.E_m.\exp \{-(\omega t-\pi)/\omega RC\} \qquad [3.13]$$

Normalised equations for V_{c1} and V_{c2} are given below

$$V_{c1n} = -1 + [1 + V_{c1n}(\pi^+)].\exp \{-(\omega t-\pi)/R_n\} \qquad [3.14]$$

$$V_{c2n} = 1.0 \qquad [3.15]$$

$$i_{sn} = -(V_{c1n} + V_{c2n})/R_n \qquad [3.16]$$

In steady state the eq.3.14 reduces the following

$$V_{c1n} = -1 + 2.\exp \{-(\omega t-\pi)/R_n\}$$

Equations 3.9 , 3.11 , 3.13 ,3.14 , 3.15 and 3.16 describe the operation doubling rectifier in Mode 2 .

Method of Solution : The equations for different modes derived above have been programmed on HP-UX 9000 using Fortran 77

language. The flow chart of this program is shown in Fig. 3.5. The transients last for one half cycle only and steady state is reached immediately after that due to the ideal nature of the source .

3.1.2 **AVERAGE OUTPUT VOLTAGE** In this section ,an expression for average output voltage has been derived . The expression for average output voltage has been derived by integrating (V_{c1} + V_{c2}) over a period from 0 to 2π .

Average output voltage ,

$$V_o = 1/2\pi.\int_0^{2\pi}(V_{c1} + V_{c2}).d(\omega t)$$

$$=1/2\pi.[\int_0^{\pi}(V_{c1} + V_{c2}).d(\omega t)+\int_{\pi}^{2\pi}(V_{c1} +V_{c2}).d(\omega t)]$$

Substitution from equations 3.1 ,3.4 ,3.9 ,3.13 gives in above equation

$$V_o = (1/\pi).2E_m.\omega.RC\ [\ 1 -\exp(-\pi/\omega RC)] \qquad [3.17]$$

Normalisation gives

$$V_{on} = 2R_n/\pi.[\ 1 - \exp(-\pi/R_n)] \qquad [3.18]$$

Average output current ,

$$I_{on} = 2/\pi.[\ 1 - \exp(-\pi/R_n)] \qquad [3.19]$$

Equations 3.18 and 3.19 give average output voltage and current .

3.1.3 **PEAK TO PEAK OUTPUT VOLTAGE RIPPLE** In this section an expression has been derived for peak to peak output voltage

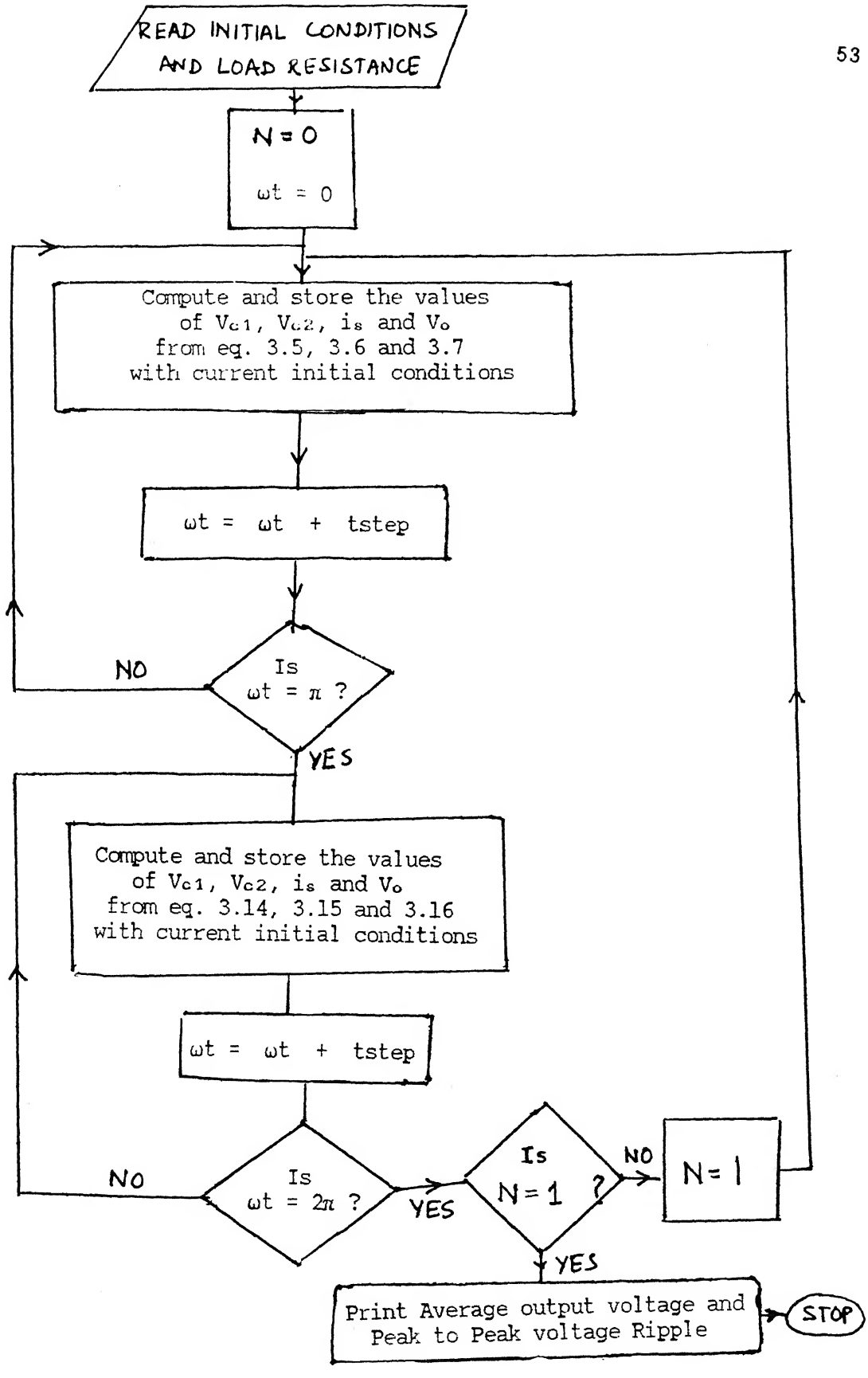


Fig.3.5 Flow chart for the Simulation of the Voltage doubling rectifier fed by ideal square

ripple. The output voltage follows a certainpattern .It reaches maximum at $\omega t = 0^{+}, \pi^{+}, 2\pi^{+}$... and touches the lowest point at $\omega t = 0^{-}, \pi^{-}, 2\pi^{-}$... That is why output voltage ripple can be calculated in the period from 0 to π or π to 2π . Typical output voltage waveform has been shown in Fig.3.1(b).

Hence Peak to Peak output voltage ripple,

$$V_{o\text{-ripple pp}} = (V_o)_{\omega t=0^{+}} - (V_o)_{\omega t=\pi^{-}}$$

$$= (V_{c2})_{\omega t=0^{+}} - (V_{c2})_{\omega t=\pi^{-}}$$

From equation 3.4 ,we have

$$= 2E_m[\ 1 - \exp(-\pi/\omega RC)\ ] \qquad [3.20]$$

Normalised peak to peak voltage ripple,

$$V_{o\text{-ripple ppn}} = 2.[\ 1 - \exp(-\pi/R_n)\ ] \qquad [3.21]$$

With all the expressions found above it is clear that variables of interest in the power doubling rectifier ,average output voltage and peak to peak output voltage ripple depend upon the value of normalised load resistance .

3.1.4 SOURCE CURRENT IMPULSE In this section , an expression for source current impulse has been found .At $\omega t = 0, \pi, 2\pi$ .. there are positive and negative source current impulses in order to supply charge to capacitor 1 & 2 respectively . These impulses raise the voltage across capacitor 1 & 2 to E_m .The strength of impulse could be found as follows :

$$\text{Impulse strength} = C.\Delta V_{c1n}$$

$$= C.\Delta V_{c2n}$$

From the expession for peak to peak output voltage ripple found above, Impulse strength = $2.[\ 1 - \exp(-\pi/R_n)\ ]$ [3.22]

3.1.5 DISCUSSION OF SIMULATION RESULTS In this section the general behaviour of the rectifier has been studied .The transient behaviour , steady state behaviour ,average output voltage and peak to peak output voltage ripple has been recorded for different values of load resistances .Fig.3.6, 2.8 and 2.9 show these respectively.The results are discussed below :

3.1.5.1 Loaded Transient and Steady State Behaviour

Fig.3.6 shows the simulated output voltage , voltage across capacitor 1 and 2 and source current ,i_s for the doubling rectifier with load resistance of 10.0 p.u.

The circuit of Fig.3.1 is excited from cold its behaviour recorded . At $\omega t = 0^+$,the diode D_1 turns on as the supply voltage ($+E_m$) is larger than capacitor 1 voltage (being zero). A source current impulse results because of this voltage difference .This voltage difference is [$E_m - V_{c1(\omega t)=0^-}$].The diode D_2 is off as the negative of supply voltage is less than voltage across capacitor 2 . With D_1 on and D_2 off the following happens :
The voltage across capacitor 1 stays at E_m and voltage across capacitor 2 starts falling from 0 to a value decided by RC .At $\omega t = \pi$,the source voltage jumps to $-E_m$ and diode D_1 turns off . The diode D_2 turns on as the negative of the supply voltage is greater than voltage across capacitor 2 .A negative source current impulse

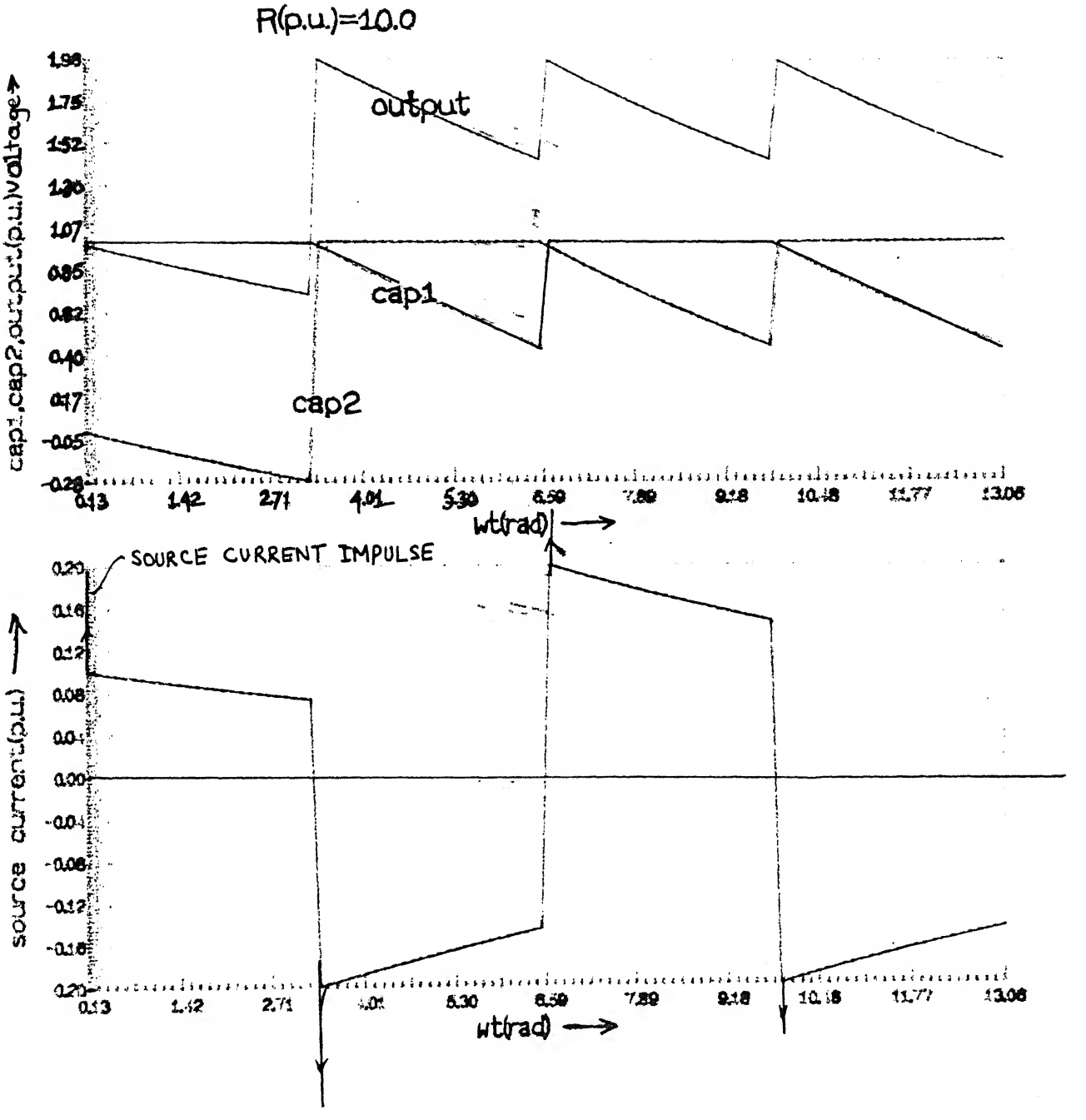


Fig.3.6 Loaded Transient Behaviour of the voltage doubling rectifier fed by an ideal square wave voltage source

flows through D_2 to supply the charge required by the capacitor 2 to acquire the voltage of E_m .A similar positive source current impulse resulted at $\omega t = 0^+$ to supply the charge to capacitor 1 to enable it acquire the voltage of $+E_m$ .The diode D_1 remains off during the period from π to 2π .The diode D_2 remains off during the period from 0 to π .

At $\omega t = 2\pi$, the diode D_2 turns off as the supply voltage jumps to $+E_m$ from $-E_m$ and from here onwards the same process repeats . So the circuit follows a sequence of D_1 on ,D_2 off and D_2 on ,D_1 off and so on .Mode transition diagram is shown in Fig.3.2 .

3.1.5.2 Average Output Voltage vs. Load Resistance (p.u.)

Average output voltage rises as the load resistance increases .The output willreach a maximum of 2.0 p.u. with load resistance infinity ,theoretically .With the increased load resistance , the capacitor 1 & 2 once charged to 1.0 p.u. at $\omega t = 0^+$& π^+ respectively do not discharge much and as a result average output voltage goes up .Fig.2.8 shows this behaviour .

3.1.5.3 Peak to Peak Output Voltage Ripple vs. Load Resistance

The peak to peak output voltage ripple decreases as the load resistance increases (Fig. 2.9).The capacitors can't lose much of their charge when the load resistance is high .So the higher the load resistance , lower will be the peak to peak voltage ripple .

3.1.5.4 Average output current follows the same pattern as that of average output voltage .

3.1.5.5 Strength of the source Current Impulse

This is directly proportional to the the peak to peak output voltage ripple and is given by $C.\Delta V_o$. Hence the effect of increased load resistance is same as that on peak to peak output voltage ripple .

3.1.5.6 When the load terminals are open circuited the following happens : Assuming we started with zero initial conditions ,at $\omega t = 0^+$,there will be an impulse of current through diode D_1 and as a result Capacitor 1 will be charged to $+E_m$ immediately . The current through diode D_1 goes to zero after the capacitor 1 has been charged to peak value for there is no parallel path across capacitor 1 .Capacitor 1 & 2 remain charged with $+E_m$ and 0 respectively in the rest of the cycle from 0 to π .

At $\omega t = \pi^+$, D_2 turns on an capacitor 2 is also charged to $+E_m$ owing to a negative source current impulse .The current through D_2 falls to zero immediately after the capacitor 2 has been charged . Capacitors 1 & 2 are thus charged to 1.0 p.u. each and output remains at 2.0 p.u. for all values of time after $\omega t = \pi^+$.The source current is also zero after $\omega t = \pi^+$.

3.2 VOLTAGE DOUBLING RECTIFIER FED BY NON IDEAL SQUARE WAVE VOLTAGE SOURCE

The doubling rectifier (Fig. 3.7) fed by non ideal square wave voltage source has three modes of operation . The non ideal square wave voltage source has resistance , R_s and reactance, ωL_s . The modes are characterized by patterns of diode conduction . The modes of operation in steady state are

Mode 1 :D_1 ON , D_2 OFF, $\alpha < \omega t \leq \beta$,$\alpha = 0$

Mode 2 :D_1 OFF, D_2 OFF, $\beta < \omega t \leq \pi$ and $\pi + \beta < \omega t \leq 2\pi$

Mode 3 :D_1 OFF, D_2 ON , $\pi < \omega t \leq \pi + \beta$

The description of each mode is as follows :

MODE 1 : The equivalent circuit for this mode is shown in Fig.3.9. In this mode the diode D_1 starts conduction at $\omega t = 0$ as the supply voltage is larger than capacitor 1 voltage . At $\omega t = 0$, a sinusoidal pulse of current flows through diode D_1 as the voltage across capacitor 1 is less than E_m .Voltage across capacitor now jumps to a value larger than E_m(decided by R-L-C series combination) from a value less than E_m as a result of this pulse of current. Diode D_1 turns off as soon as the source current becomes zero. The circuit enters Mode 2 at $\omega t = \beta$. The voltage across capacitor 2 falls.

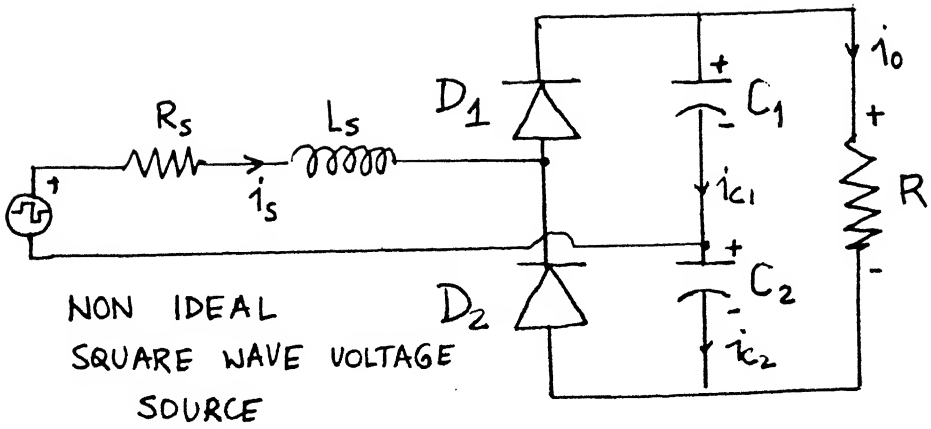


Fig.3.7 Voltage Doubling Rectifier fed by Non ideal Square wave voltage source.

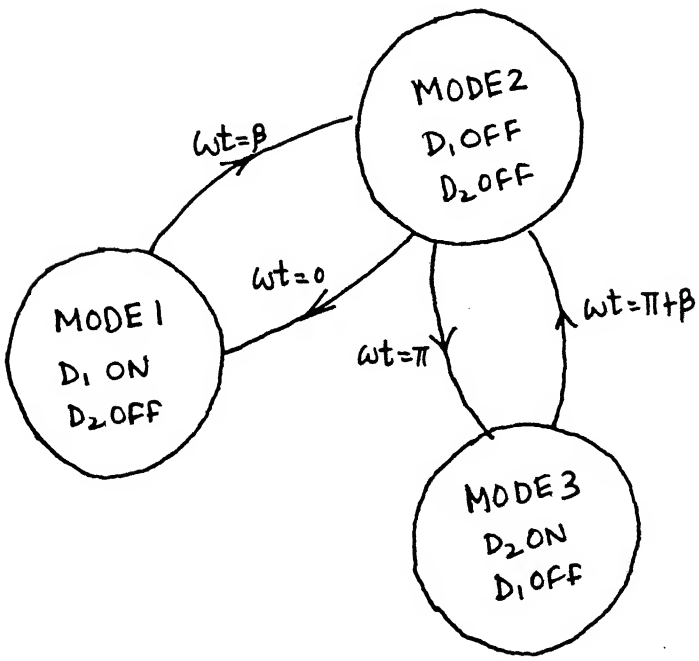


Fig.3.8 Mode transition diagram in the steady state

MODE 2 : The equivalent circuit for this mode is shown in Fig.3.10. The circuit enters mode 2 at $\omega t = \beta$. In this mode both the diodes are off as they are reverse biased. Voltage across both the capacitors fall as they supply energy to the load.

MODE 3 : The equivalent circuit for this mode is shown in Fig.3.11. The circuit enters mode 3 at $\omega t = \pi$ as the negative of the supply voltage is larger than the voltage across capacitor 2 or in other words diode D_2 gets forward biased. The voltage across capacitor 2 rises to a value larger than E_m due to a negative source current pulse at $\omega t = \pi$. The voltage across capacitor 1 falls in this mode.

The circuit again enters mode 2 at $\omega t = \pi + \beta$ as the source current becomes zero. The diodes D_1 and D_2 remain off in this mode and the load is supplied by the stored energy in the capacitors. At $\omega t = 2\pi$, the mode 1 starts again and the same process repeats. Mode transition diagram in steady state is shown in Fig.3.8.

3.2.1 DIFFERENTIAL EQUATIONS OF THE DOUBLING RECTIFIER FOR MODES 1, 2 AND 3

In this section the differential equations describing the rectifier in different modes have been written . The derivatives of voltage across capacitors 1 & 2 and source current have been used in simulating the behaviour of the doubling rectifier . The

three variables of interest are V_{c1} , V_{c2} and i_s . The reference direction of capacitor voltage and current and source current are shown in the Fig. 3.7 . The equations have been normalised as per the normalisation scheme given in the beginning of the chapter . The diodes have been assumed to be ideal. The pattern of modes in steady state is 1, 2, 3, 2, 1, 2 ... . The mode transition diagram is given in Fig. 3.8 .

Mode 1 (Fig. 3.4) : In this mode D_1 is on and D_2 is off . Source current is positive . The circuit enters Mode 1 at $\omega t = 0$. The three differential equations are

$$E_m = i_s.R_s + L_s.d(i_s)/dt + V_{c1} \qquad [3.22]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c2})/dt \qquad [3.23]$$

$$\text{source current}, i_s = C.d(V_{c1})/dt + (V_{c1} + V_{c2})/R \qquad [3.24]$$

Normalising the above equations , we have from equation 3.22

$$1.0 = i_s.R_s/E_m + (L_s/E_m).[d(i_s)/dt] + V_{c1}/E_m$$

$$1.0 = (i_s.R_s.\omega C)/(E_m.\omega C) + (L_s.\omega^2 C)/(E_m.\omega C).[d(i_s)/d(\omega t)] + V_{c1}$$

$$1.0 = i_{sn}.R_{sn} + (\omega L_s)_n.\left[\frac{d(i_s)_n}{d(\omega t)}\right] + V_{c1n} \qquad [3.25]$$

From equation 3.22

$$(V_{c1} + V_{c2})/E_m = - (RC/E_m).d(V_{c2})/dt$$

$$V_{c1n} + V_{c2n} = - (RC.\omega)/(E_m).d(V_{c2})/d(\omega t)$$

$$V_{c1n} + V_{c2n} = - R_n.\left[\frac{dV_{c2n}}{d(\omega t)}\right] \qquad [3.26]$$

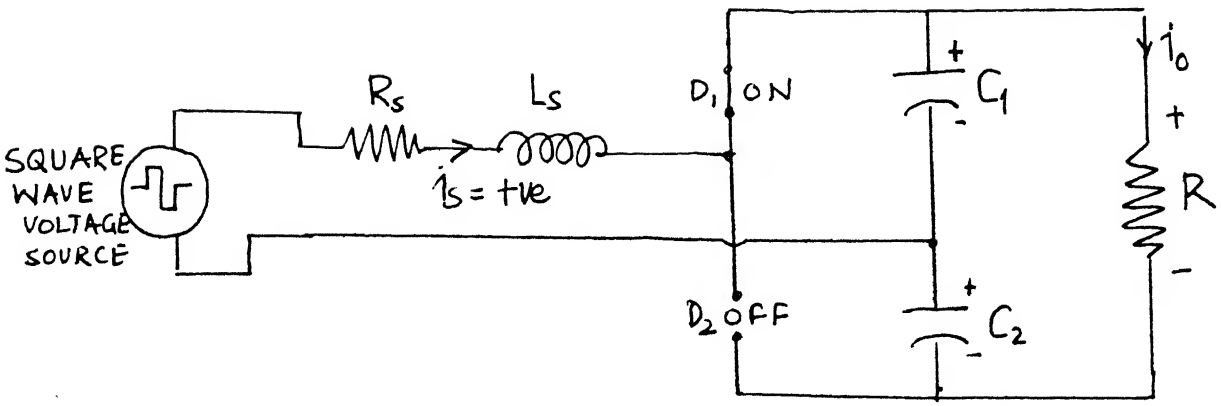


Fig.3.9 Equivalent circuit in Mode 1.

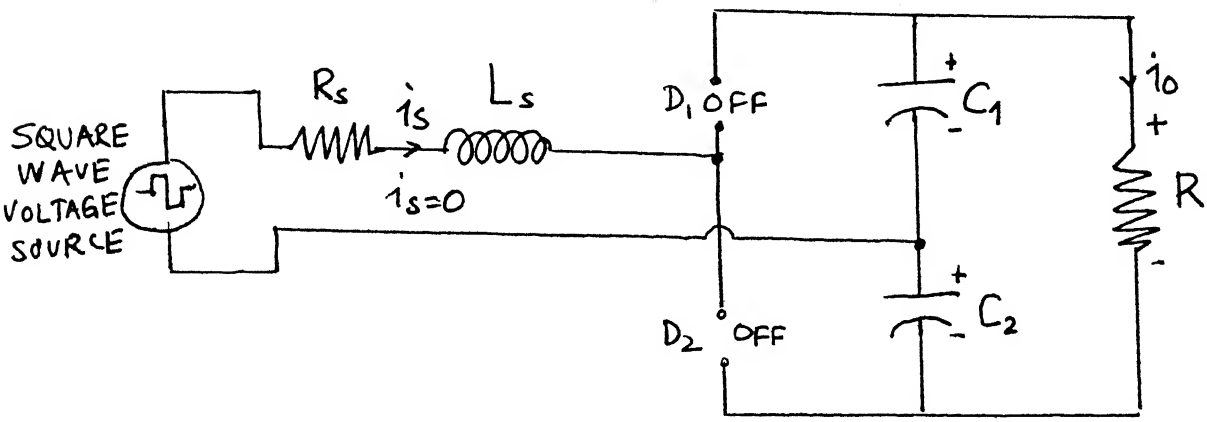


Fig.3.10 Equivalent circuit in Mode 2.

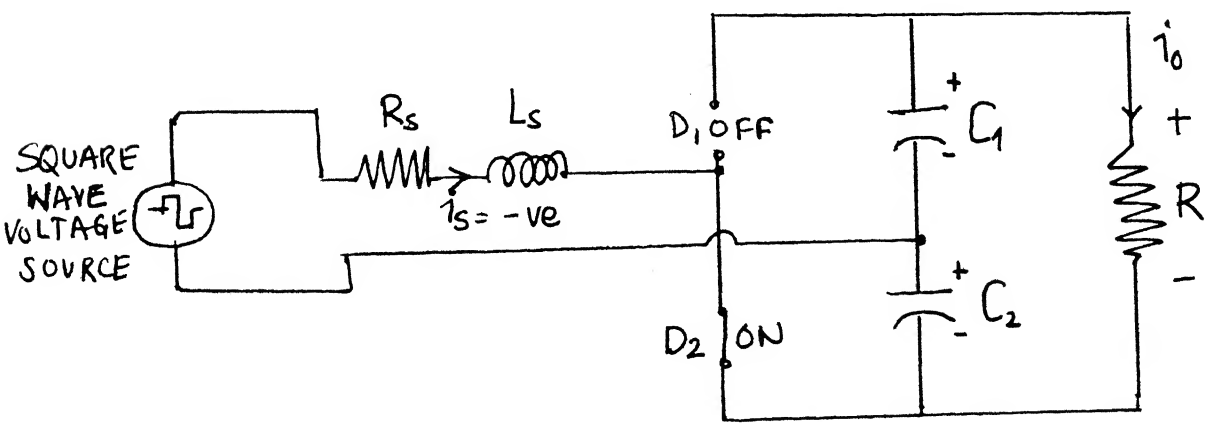


Fig.3.11 Equivalent circuit in Mode 3.

From equation 3.24

$$i_s/(E_m.\omega C) = C/(E_m.\omega C).d(V_{c1})/dt + (V_{c1} + V_{c2})/(R.E_m.\omega C)$$

$$i_{sn} = \left[\frac{d(V_{c1})_n}{d(\omega t)}\right] + \frac{(V_{c1n} + V_{c2n})}{R_n} \qquad [3.27]$$

In all the equations derived above suffix n represents normalised variables e.g. $(\omega L_s)_n = \omega^2.L_s.C$ represents normalised source reactance .

Equations 3.22, 3.23, 3.24, 3.25, 3.26 and 3.27 describe the operation of voltage doubling rectifier in Mode 1 .

MODE 2 (Fig. 3.10) : In this mode both the diodes D_1 and D_2 are off . The circuit is characterised by source current , $i_s = 0$ .The circuit enters mode 2 at $\omega t = \beta$ when source current becomes zero . The three differential equations are

$$\text{source current }, i_s = 0 \qquad [3.28]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c2})/dt \qquad [3.29]$$

$$(V_{c1} + V_{c2}) / R = -C.d(V_{c1})/dt \qquad [3.30]$$

Normalised equations can be written as follows

$$i_{sn} = 0 \qquad [3.31]$$

Equations 3.29 and 3.30 are of the kind of equation 3.23 , hence the normalised equations can be directly written as

$$V_{c1n} + V_{c2n} = - R_n.\left[\frac{dV_{c1n}}{d(\omega t)}\right] \qquad [3.32]$$

$$V_{c1n} + V_{c2n} = - R_n . \left[\frac{dV_{c2n}}{d(\omega t)} \right] \qquad [3.33]$$

Equations 3.28, 3.29, 3.30, 3.31, 3.32 and 3.33 describe the operation of the doubling rectifier in mode 2 .

MODE 3 (Fig. 3.11) : In this mode diode D_1 is off and diode D_2 is on . The circuit enters mode 3 at $\omega t = \pi$ when negative of the supply voltage becomes greater than voltage across capacitor 2. The source current is negative . The three differential equations of the circuit are derived below

$$- E_m = i_s . R_s + L_s . d(i_s)/dt - V_{c2} \qquad [3.34]$$

$$(V_{c1} + V_{c2}) / R = - C . d(V_{c1})/dt \qquad [3.35]$$

$$\text{source current}, i_s = - C . d(V_{c2})/dt - (V_{c1} + V_{c2})/R \qquad [3.36]$$

Normalisation of the equations can be done as earlier and the resulting equations in per unit are given below

$$- 1.0 = i_{sn} . R_{sn} + (\omega L_s)_n . \left[\frac{d(i_s)_n}{d(\omega t)} \right] - V_{c2n} \qquad [3.37]$$

$$V_{c1n} + V_{c2n} = - R_n . \left[\frac{dV_{c1n}}{d(\omega t)} \right] \qquad [3.38]$$

$$i_{sn} = \left[\frac{d(V_{c1})_n}{d(\omega t)} \right] + \frac{(V_{c1n} + V_{c2n})}{R_n} \qquad [3.39]$$

Equations 3.34, 3.35, 3.36, 3.37, 3.38 and 3.39 describe the operation of the doubling rectifier in mode 3 .

3.2.2 The method of computation of numerical average output voltage and peak to peak output voltage ripple from the data points (instantaneous values of V_{c1}, V_{c2} and i_s over 2π radians in steady state) is similar to that given in sec. 2.2.2.

3.2.3 DISCUSSION OF SIMULATION RESULTS In this section the general behaviour of the doubling rectifier has been studied . The transient behaviour,steady state behaviour,average output voltage and peak to peak voltage ripple for different values of load resistances and source reactances have been calculated and shown in Figs.3.13, 3.14 and 3.15. These results are discussed below :

3.2.3.1 LOADED TRANSIENT AND STEADY STATE BEHAVIOUR OF THE DOUBLING RECTIFIER FED BY NON IDEAL SQUARE WAVE VOLTAGE SOURCE

The circuit of Fig. 3.7 with a load resistance of 10.0 p.u. , source resistance of 0.01 p.u. and source inductive reactance of 0.05 p.u. was simulated for studying its transient and steady state behaviour.

Fig. 3.12 shows the simulated output voltage, voltage across capacitor 1, voltage across cpacitor 2, source current and input voltage. The circuit was excited from cold and behaviour recorded.

At $\omega t = 0^+$, the diode D_1 turns on as the supply voltage is more than the voltage across capacitor 1. Capacitor 1 voltage at $\omega t = 0^+$ is zero as the circuit is excited from cold. Diode D_2 is

off as it is reverse biased by the supply voltage. Difference in supply voltage & the voltage across capacitor 1 at $\omega t = 0^+$ causes a large sinusoidal current pulse. This pulse tends to become an impuse as the value of source reactance reduces. Due to this large pulse the voltage across capacitor 1 jumps to approximately 1.8 p.u.

During this period when diode D_1 is on diode D_2 is off, voltage across capacitor 2 increses in the negative direction as at the start of this interval the voltage across capacitor 2 was zero.

The diode D_1 turns off soon as the source current becomes zero and the circuit enters mode 2. In this mode of operation, since the voltage across capacitor 1 is more than 1.0 p.u., D_1 remains off and D_2 was already off. The two capacitors supply energy to the load and thus the output voltage falls. The voltage across capacitor 2 further increases in the negative direction and touches -0.42 p.u. The voltage across capacitor 1 decreases from the level of 1.8 p.u. to approximately 1.5 p.u.

Again at $\omega t = \pi$, there appears a large negative source current pulse. The amplitude of this pulse is much larger as compared to the pulse generated at $\omega t = 0^+$, the reason being the large difference in voltage across cpacitor 2 and the negative of the supply. The voltage across capacitor 2 at $\omega t = \pi$ actually adds to E_m and causes this current pulse which raises the voltage across capacitor 2 to about 2.2 p.u. The rise in the voltage is larger than the rise in the voltage across capacitor 1 at $\omega t = 0$. The source current soon crosses zero and diode D_2 turns off. D_1

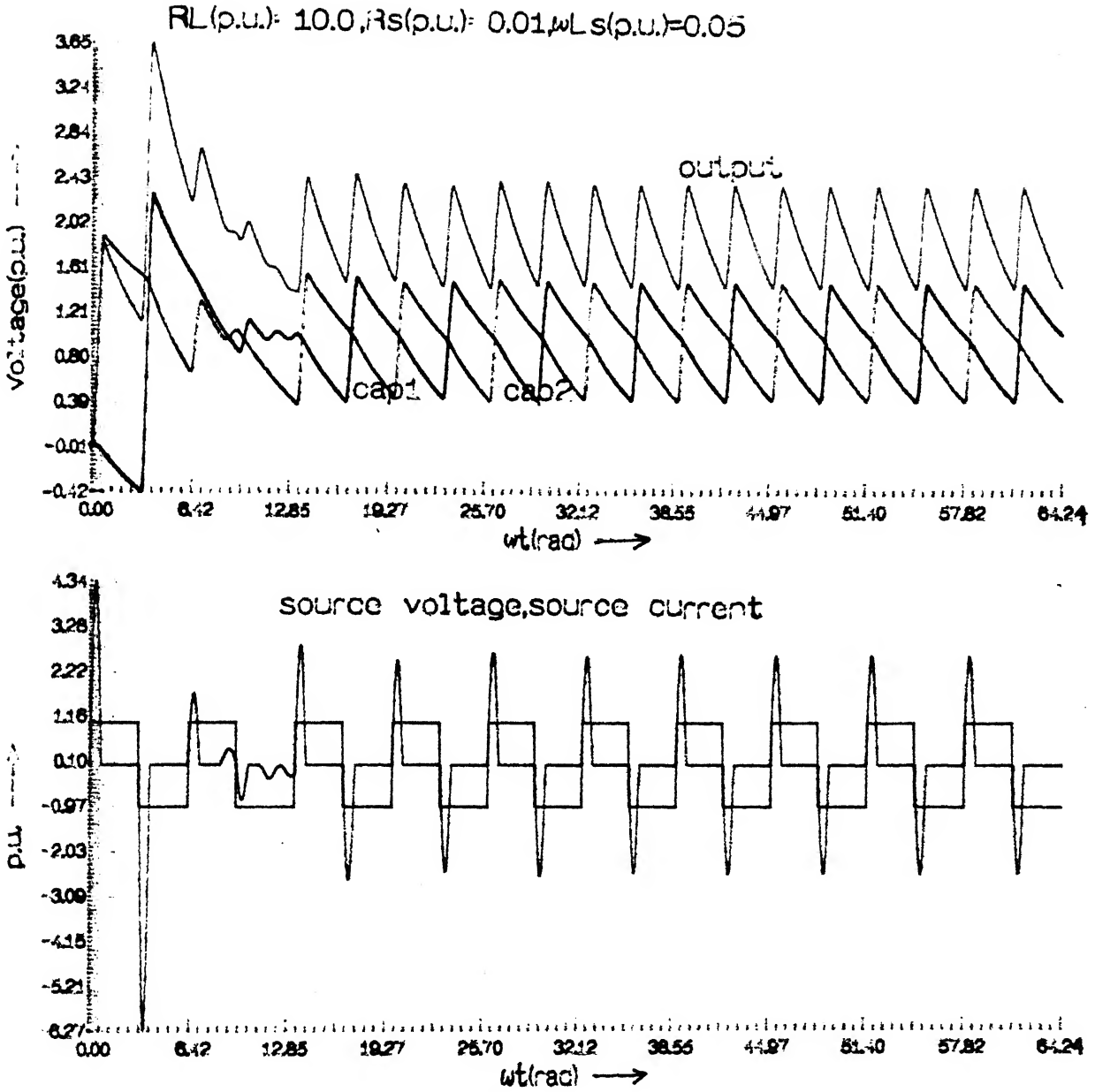


Fig.3.12 Loaded transient behaviour of the voltage doubling rectifier fed by non ideal square wave voltage source

was off as it was reverse biased by the supply voltage. In this mode both the diodes are off and capacitors supply energy to the load. The circuit remains in this mode till $\omega t = 2\pi$

MULTIPLE CONDUCTION OF THE DIODES DURING TRANSIENT PERIOD

Multiple conduction of the diodes is a phenomenon in which the diode D_1/D_2 conducts more than once in the positive/negative half cycles of the input supply.Multiple conduction of the diode D_1 is noticed in the period from $\omega t = 2\pi$ to 3π. Multiple conduction of the diode D_2 is noticed in the period from $\omega t = 3\pi$ to 4π. Multiple conduction occurs because of the fact that the diode D_1/D_2 gets forward biased more than once in the positive/negative half cycles of the supply.

In the period from $\omega t = 2\pi$ to 3π, the supply voltage is 1.0 p.u. At the start of the interval there was a source current pulse and the voltage across cpacitor 1 rose to 1.3 p.u. Soon after the voltage rose to 1.3 p.u., Diode D_1 went off and the voltage across capacitor 1 started falling and became equal to 1.0 p.u. This forward biased the diode D_1 and it conducted again, second time, in the positive half cycle.

Similar arguments apply for the explanation of the multiple conduction of D_2 in the negative half cycle from $\omega t = 3\pi$ to 4π.

The circuit reaches steady state approximately after 4π radians. In the staedy state, however, multiple conduction does not occur. In steady state the diodes conduction patterns is as

3.2.3.4 Variation of the average output voltage with load resistance and source reactance

Average output voltage vs. source reactance :

The characteristics is shown in Fig. 3.14. From Fig. it is clear that the average output voltage falls both at very low values of ωL_s and at at relatively large values of ωL_s. The average output voltage is close to the ideal value of 2.0 p.u. for the range of ωL_s = 0.15 to 0.7.

From the wave forms of the Fig.3.13 , the source current is seen to have sharp sinusoidal pulses at ωL_s = 0.05 p.u. As ωL_s reduces towards ideal value of zero, these tend to become impulses as analysed in section in 3.1. Due to these sharp pulses of source current, the diodes D_1 and D_2 turn off after conducting for very short intervals of time in the positive and negative half cycles respectively.Therefore the capacitors supply energy to the load for most part of the cycle and thus output voltage falls for most part of the cycle. The average output voltage, hence, is low at low values of ωL_s.

At high values of ωL_s (> 0.7 p.u.) the peak source current reduces and due to large values of the source reactance the conduction period of the diodes in the positive and negative half cycles increases. However, the average output voltage falls as the inductive circuit is not able to transfer charge quickly.

Average output voltage vs. load resistance :

The average output voltage rises as the load resistance is

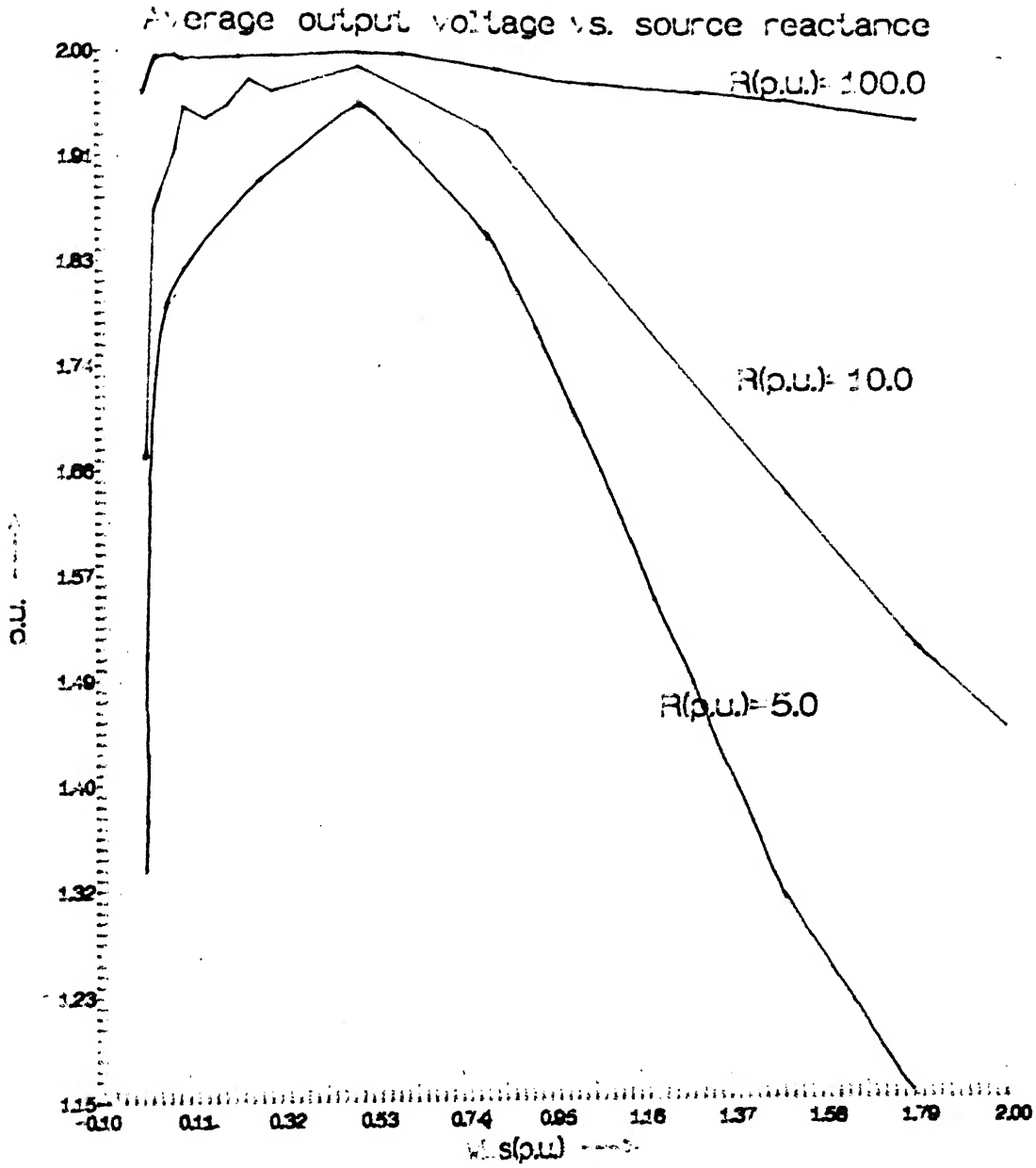


Fig.3.13 "Average output voltage Vs Source Reactance characterstics" for varying Load Rresistances for the voltage doubling rectifier fed by nonideal square wave voltage source

increased. With the increased load resistance, the capacitors do not lose much of their stored energy and as a result the output voltage rises.

3.2.3.5 Variation of the Peak to Peak Output Voltage Ripple with load resistance and source reactance

Peak to Peak Output Voltage ripple vs. Source reactance:

The characteristics is shown in Fig. 3.15. As explained in sec.3.2.3.4 above, the ripple voltage reduces as the source reactance is increased. At low values of the ωL_s, the diodes conduct large current pulses for shorter durations. These large current pulses cause sharp voltage rises across capacitors 1 & 2. For most part of the cycle diodes are off and capacitors discharge from their peak levels causing a large peak to peak output voltage ripple.

At large values of source reactances, the conduction period of the diodes increase and the ripple in output voltage reduces.

Peak to Peak output voltage ripple vs. load resistance:

The peak to peak output voltage ripple reduces as the load resistance is increased. This is so because the capacitors' voltage fall is less at higher values of the load resistances.

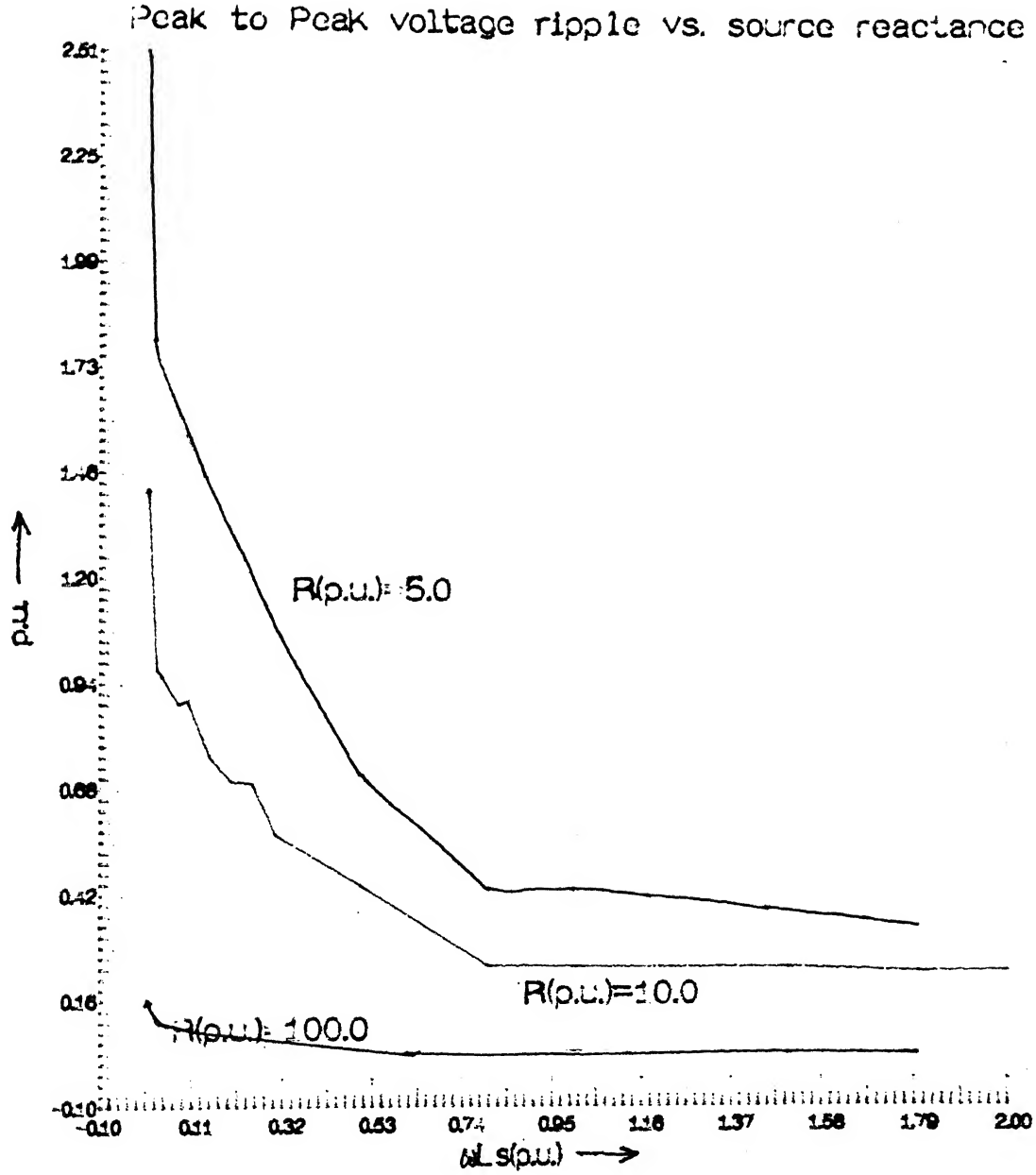


Fig.3.14 "Peak to Peak output voltage ripple Vs Source Reactance characterstics" for varying Load Resistances for the voltage doubling rectifier fed by nonideal square voltage source

CHAPTER 4

CAPACITOR DIODE MULTIPLIER FED BY CURRENT SOURCES

In this chapter, capacitor-diode voltage multiplier fed by square wave and sine wave current sources has been studied . Analysis is based on the differential equations modelling of the multiplier in its different modes of operation .Differential equations have been programmed and simulation results presented.

4.1 CAPACITOR-DIODE MULTIPLIER FED BY AN IDEAL SINE WAVE AND SUARE WAVE CURRENT SOURCES

The multiplier (Fig.4.1a and 4.1b) has two modes of operation characterised by the patterns of diodes conduction shown in Fig. 4.2 . The modes are

Mode 1 : D_1 on , D_2 off $\quad 0 < \omega t \leq \pi$

Mode 2 : D_2 on , D_1 off $\quad 0 < \omega t \leq 2\pi$

MODE 1 : In this mode ,the diode D_1 conduct sand D_2 remains off as the supply current is positive . The positive source current finds the path through capacitor 1 & 2 and the load resistance as shown in the Fig. 4.3 & 4.9 . The mode exists from $\omega t = 0$ to π i.e. during the period when source current is positive .

MODE 2 : In this mode ,the diode D_2 conducts and D_1 remains off as the source current is negative. The negative source current finds

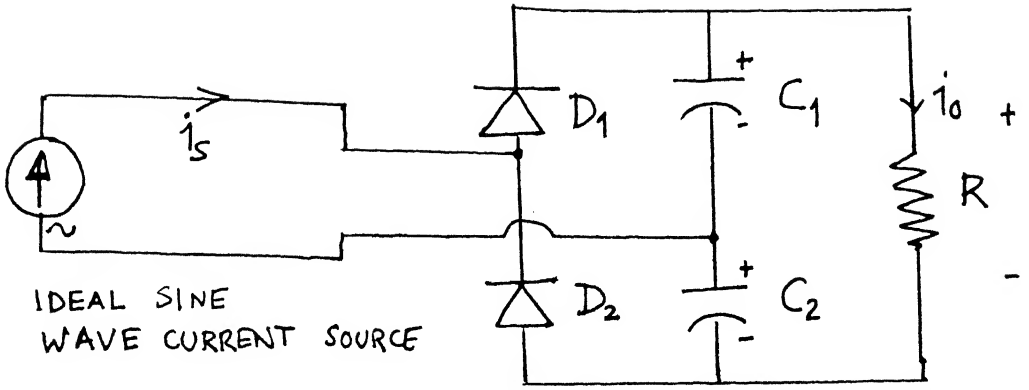


Fig.4.1(a) Capacitor Diode Voltage Multiplier fed by an ideal sine wave current source.

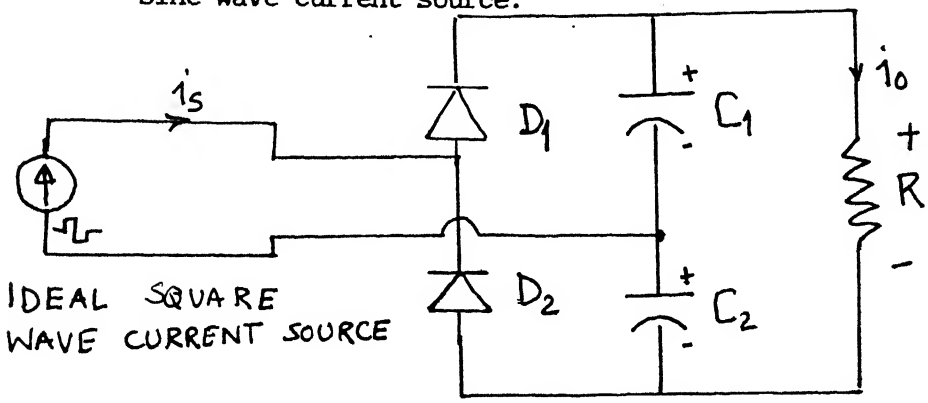


Fig.4.1(b) Capacitor Diode Voltage Multiplier fed by an ideal square wave current source.

path through D_2 and flows through capacitors 1 & 2 and load resistance as shown in Fig. 4.4 and 4.10 . The mode exists from $\omega t = \pi$ to 2π i.e. during the period when source current is negative . Cyclic changes in the modes of operation is shown in the Fig.4.2 . The patterns of modes is 1 , 2 , 1 .....and so on .

4.2 DIFFERENTIAL EQUATIONS FOR THE CAPACITOR - DIODE MULTIPLIER FED BY IDEAL SINE WAVE CURRENT SOURCE

In this section the differential equations describing the capacitor diode multiplier in its modes of operation have been derived . The equations have been converted in p.u. form as per the normalisation scheme given below :

Normalisation Scheme : The applied sine wave current source is $i_m \sin(\omega t)$. Amplitude i_m is taken as the base current . Base impedance (similar to the normalisation scheme chosen in earlier chapters) is $1/\omega C$. Hence the base voltage is $i_m/\omega C$. Normalised variables have been represented by suffix n .

Mode 1 (Fig. 4.3) : This mode exists from 0 to π . Diode D_1 is on and D_2 is off . The diffeential equations are

$$i_m.\sin(\omega t) = C.d(V_{c1})/dt + (V_{c1} + V_{c2})/ R \qquad (4.1)$$

$$- C.d(V_{c2})/dt = (V_{c1} + V_{c2})/ R \qquad (4.2)$$

Normalising the above equations as per the scheme given above

$$\sin(\omega t) = (\omega C/i_m).d(V_{c1})/d(\omega t) + \{(V_{c1} + V_{c2}).\omega C\}/(R.i_m.\omega C)$$

$$\sin(\omega t) = \left[\frac{dV_{c1n}}{d(\omega t)}\right] + (V_{c1n} + V_{c2n})/R_n \qquad (4.3)$$

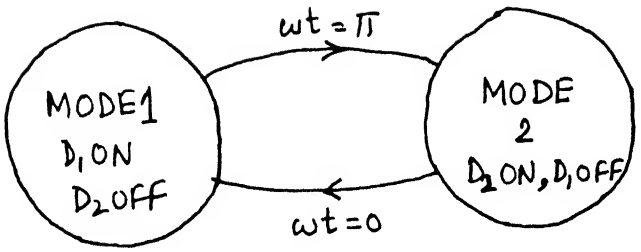


Fig.4.2 Mode Transition diagram for the capacitor diode multiplier fed by sine and square wave voltage sources

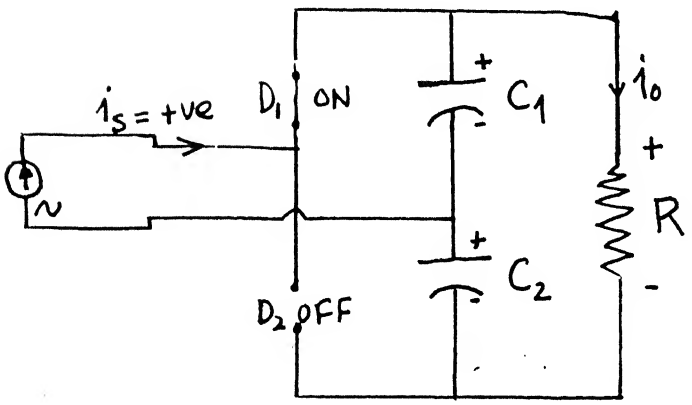


Fig.4.3 Equivalent circuit in Mode 1.

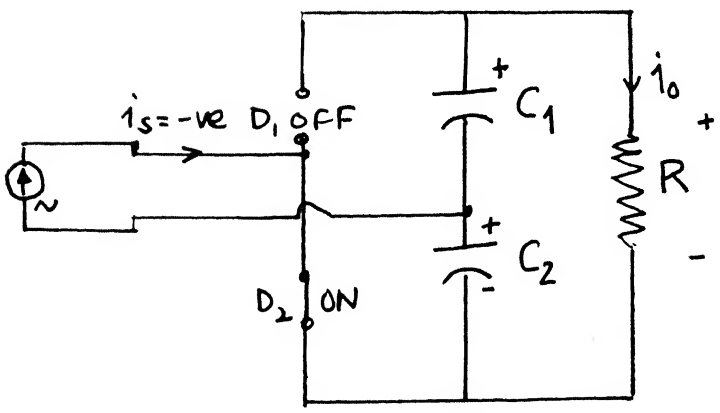


Fig.4.4 Equivalent circuit in Mode 2.

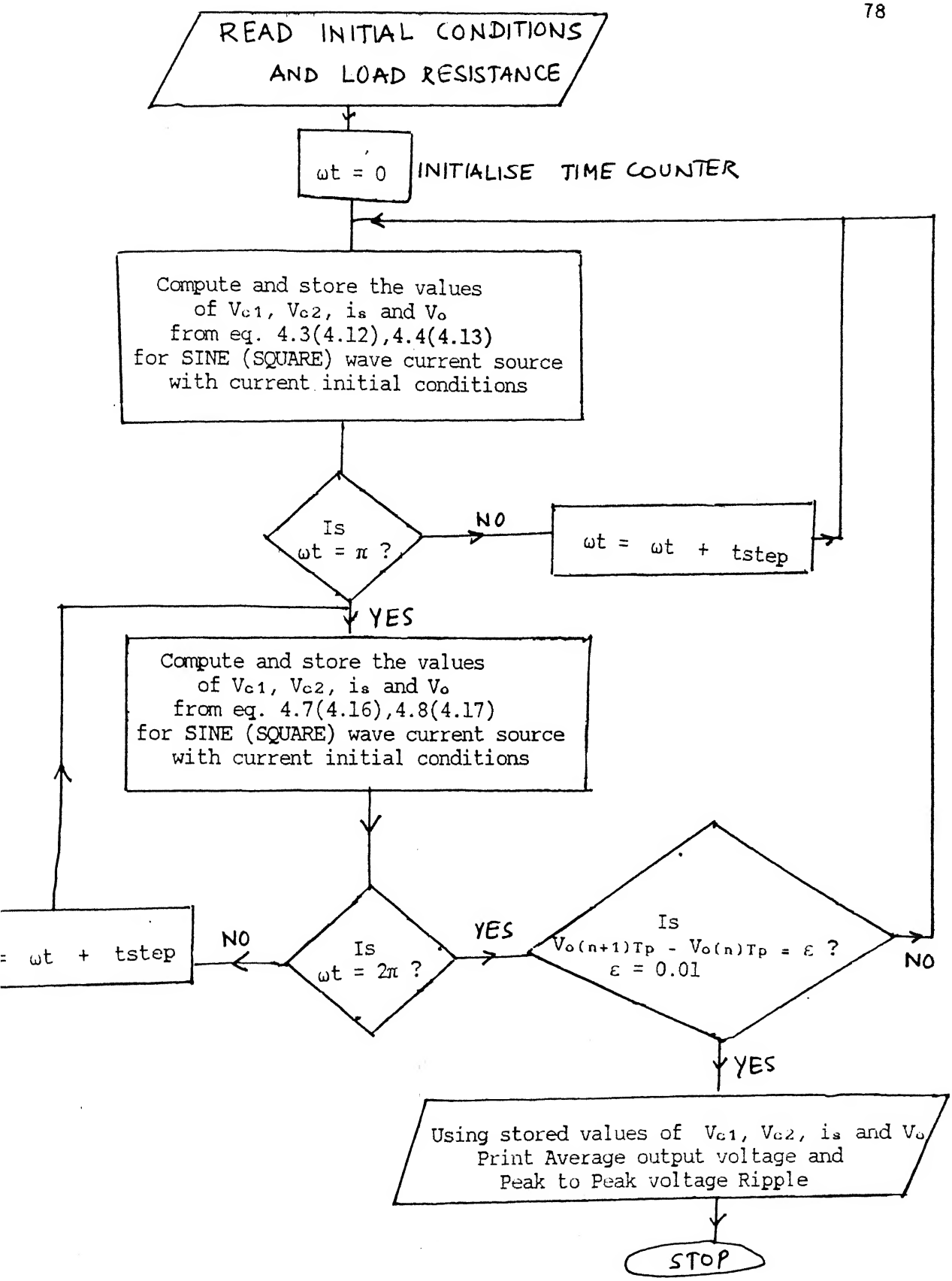


Fig.4.5 Flow chart for Simulation of the capacitor diode multiplier fed by sine and square wave current source

$$-(C.\omega)/i_m.\left[\frac{dV_{c2}}{d(\omega t)}\right] = \{(V_{c1} + V_{c2}).\omega C\}/(R.i_m.\omega C)$$

$$-\left[\frac{dV_{c2n}}{d(\omega t)}\right] = (V_{c1n} + V_{c2n})/R_n \qquad (4.4)$$

Equations 4.1 , 4.2 , 4.3 and 4.4 describe the operation of capacitor - diode multiplier fed by sine wave current source in mode 1 .

Mode 2 (Fig. 4.4) : This mode exists from $\omega t = \pi$ to 2π .In this mode D_2 is on and D_1 is off . The two differential equations are

$$i_m.\sin(\omega t) + C.d(V_{c2})/dt + (V_{c1} + V_{c2})/ R = 0 \qquad (4.5)$$

$$-C.d(V_{c1})/dt = (V_{c1} + V_{c2})/ R \qquad (4.6)$$

Normalising the above equations as per the scheme given above

$$\sin(\omega t) + (\omega C/i_m).d(V_{c2})/d(\omega t) + \{(V_{c1} + V_{c2}).\omega C\}/(R.i_m.\omega C) = 0$$

$$\sin(\omega t) + \left[\frac{dV_{c2n}}{d(\omega t)}\right] + (V_{c1n} + V_{c2n})/R_n = 0 \qquad (4.7)$$

and

$$-\left[\frac{dV_{c1n}}{d(\omega t)}\right] = (V_{c1n} + V_{c2n})/R_n \qquad (4.8)$$

Equations 4.5 , 4.6 , 4.7 and 4.8 describe the operation of the multiplier in Mode 2 .

4.3 DIFFERENTIAL EQUATIONS FOR THE CAPACITOR - DIODE MULTIPLIER FED BY AN IDEAL SQUARE WAVE CURRENT SOURCE

In this section differential equations describing the

multiplier in its modes of operation have been derived . The equations have been converted in p.u. form as per the normalisation scheme in which peak current i_m has been taken as the base current . Other base quantities are same as that taken in last section . Normalised variables are denoted by suffix n .

MODE 1 (Fig. 4.9) : This mode exists from 0 to π . Diode D_1 is on and D_2 is off .The differential equations can be written as follows

$$i_m = C.d(V_{c1})/dt + (V_{c1} + V_{c2})/ R \qquad (4.10)$$

$$- C.d(V_{c2})/dt = (V_{c1} + V_{c2})/ R \qquad (4.11)$$

Normalising the above equations as per the scheme given above

$$1.0 = (\omega C/i_m).d(V_{c1})/d(\omega t) + \{(V_{c1} + V_{c2}).\omega C\}/(R.i_m.\omega C)$$

$$1.0 = \left[\frac{dV_{c1n}}{d(\omega t)}\right] + (V_{c1n} + V_{c2n})/R_n \qquad (4.12)$$

$$- (C.\omega)/i_m.\left[\frac{dV_{c2n}}{d(\omega t)}\right] = \{(V_{c1} + V_{c2}).\omega C\}/(R.i_m.\omega C)$$

$$- \left[\frac{dV_{c2n}}{d(\omega t)}\right] = (V_{c1n} + V_{c2n})/R_n \qquad (4.13)$$

Equations 4.10 , 4.11 , 4.12 and 4.13 describe the operation of capacitor - diode multiplier fed by square wave current source in mode 1 .

Mode 2 (Fig. 4.10) : This mode exists from $\omega t = \pi$ to 2π .In this mode D_2 is on and D_1 is off . The two differential equations are

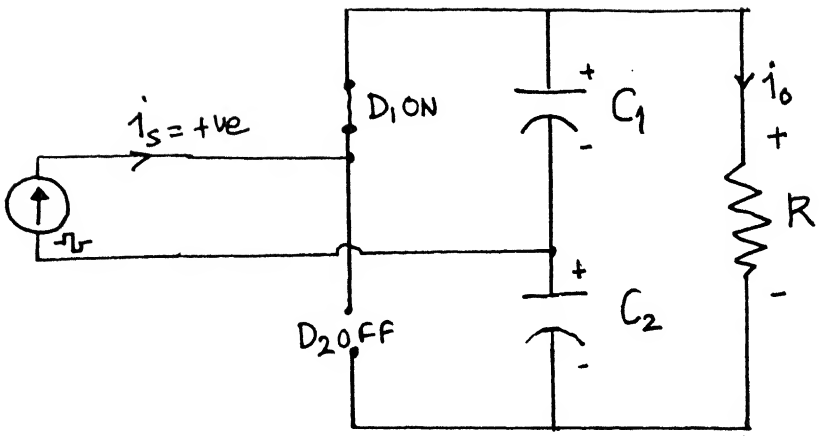


Fig.4.9 Equivalent circuit in Mode 1.

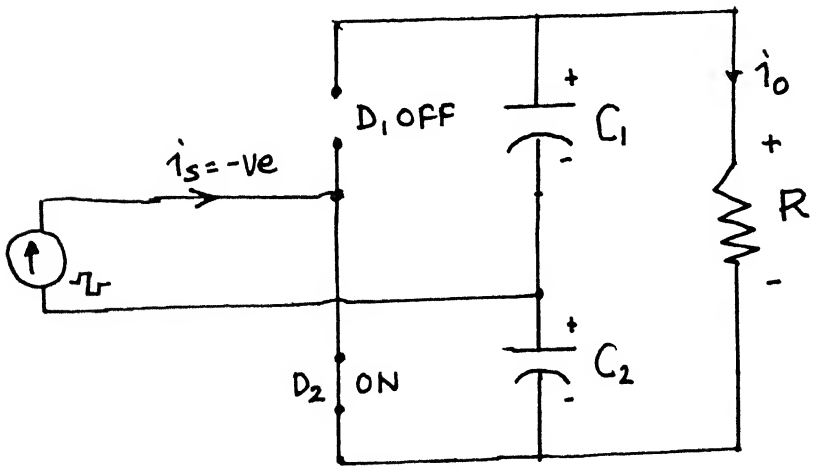


Fig.4.10 Equivalent circuit in Mode 2.

$$- i_m + C.d(V_{c2})/dt + (V_{c1} + V_{c2})/ R = 0 \qquad (4.14)$$

$$- C.d(V_{c1})/dt = (V_{c1} + V_{c2})/ R \qquad (4.15)$$

Normalising the above equations as per the scheme given above

$$-1.0 + (\omega C/i_m).d(V_{c2})/d(\omega t) + \{(V_{c1} + V_{c2}).\omega C\}/(R.i_m.\omega C) = 0$$

$$-1.0 + \left[\frac{dV_{c2n}}{d(\omega t)}\right] + (V_{c1n} + V_{c2n})/R_n = 0 \qquad (4.16)$$

and

$$- \left[\frac{dV_{c1n}}{d(\omega t)}\right] = (V_{c1n} + V_{c2n})/R_n \qquad (4.17)$$

Equations 4.14 , 4.15 , 4.16 and 4.17 describe the operation of the multiplier in Mode 2.

4.4 METHOD OF SOLUTION

The differential equations obtained for Mode 1 and Mode 2 have been solved numerically on computer using D02BAF SUBROUTINE from NAG library . The values of voltages across capacitor 1 & 2 and source current have been computed at a sufficiently large no. of points over a period from 0 to π in mode 1 and π to 2π for mode 2. The computed values (herein after reffered to as data points) have been stored appropriately to be used later for computing average output voltage and peak to peak output voltage ripple . The flowchart for the program is shown in Fig. 4.5 . The transient behaviour has been recorded from zero initial conditions and steady state is reached after a few cycles .

4.4.1 METHOD OF COMPUTATION OF AVERAGE OUTPUT VOLTAGE AND PEAK TO PEAK OUTPUT VOLTAGE RIPPLE

This is computed in the manner as follows:

The data points are available every 'tstep' radians . 'tstep' is the step size . We assume the output voltage to remain constant over 'tstep' radians .The smaller the value of 'tstep' ,higher will be the computational accuracy . Hence the average output voltage in per unit is

$$V_{oavgn} = \sum_{i=1}^{k} \frac{(V_{c1ni} + V_{c2ni})}{k}$$

k = no. of data points in a period of 2π radians .

In the complete process of transient and steady state there can be pk data points where p is a large no. Only last k datapoints are retained for these are the datapoints in which steady state has been reached . The datapoints during the transient state are only needed for plotting .The maximum and minimum values of the output voltage are picked and the difference is outputed as peak to peak output voltage ripple .

4.5 DISCUSSION OF SIMULATION RESULTS

In this section the transient and steady state behaviour of the rectifier has been recorded . Later in the section is studied the variation of output voltage and peak to peak output voltage ripple with load resistance .

4.5.1 LOADED TRANSIENT AND STEADY STATE BEHAVIOUR OF THE MULTIPLIER FED BY AN IDEAL SINE WAVE CURRENT SOURCE

Fig. 4.6 shows the simulated output voltage , voltage across capacitor 1 , capacitor 2 and applied sinusoidal input

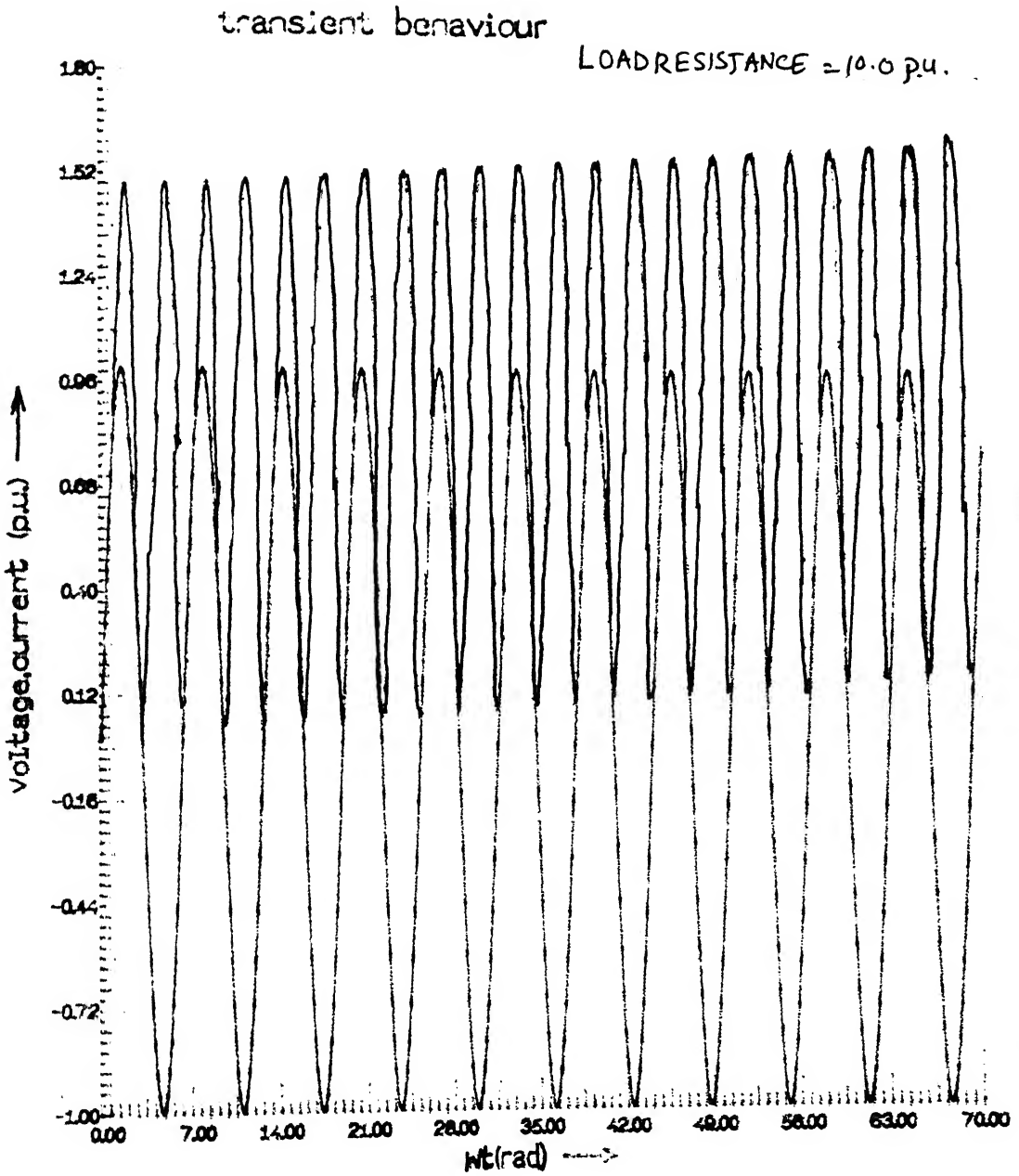


Fig.4.6(b) Transient behaviour of the capacitor diode multiplier fed by sine wave current source

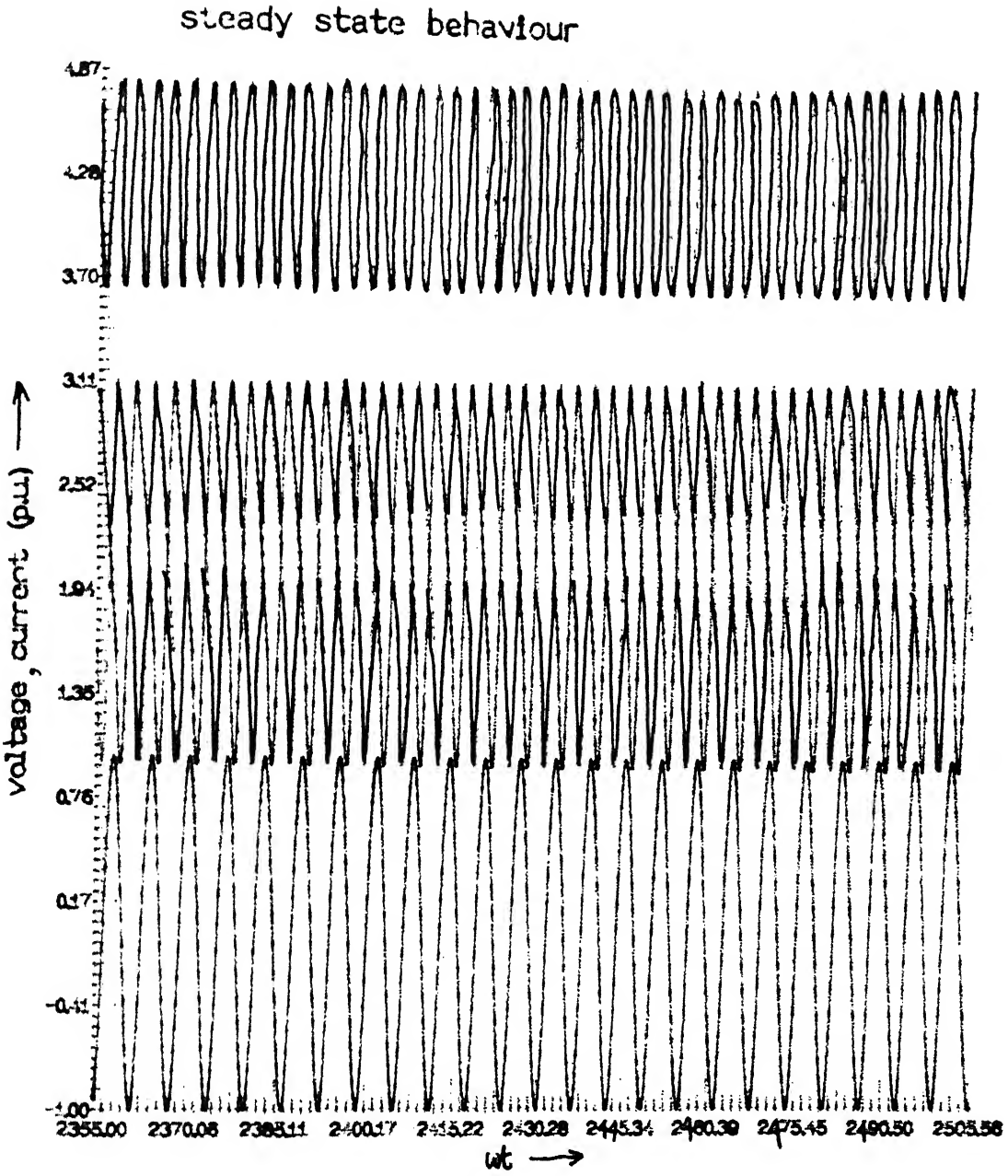


Fig.4.6(a) steady state behaviour of the capacitor diode multiplier fed by sine wave current source

current source for the multiplier having load resistance of 10.0 p.u.The circuit of Fig. 4.1a is excited from cold and the behaviour is recorded . The circuit has two modes (as already explained in the beginning of the chapter)of operation .

Mode 1 : The capacitor 1 charges and capacitor 2 discharges (actually it charges in the negative direction) during this mode.The voltage across capacitor 1 & 2 is almost sinusoidal .

Mode 2 : The reverse is true for mode 2 i.e. capacitor 2 charges and capacitor 1 discharges .The voltage across capacitor 1 & 2 are almost sinusoidal .

Slowly the capacitors 1 & 2 build some charge in them and steady state is reached after a certain no. of cycles .The voltage across capacitors 1 & 2 has a D.C. component and a 100 Hz ripple . The D.C. components add to give the average output voltage .The a.c. components have a phase difference but do not cancel each other exactly as in the square wave case .

4.5.2 LOADED TRANSIENT AND STEADY STATE BEHAVIOUR OF THE MULTIPLIER FED BY AN IDEAL SQUARE WAVE CURRENT SOURCE

Fig. 4.11 shows the simulated output voltage , voltage across capacitor 1 , capacitor 2 and applied square wave input current source for the multiplier having load resistance of 10.0 p.u.The circuit of Fig. 4.1a is excited from cold and the behaviour is recorded . The circuit has two modes (as already explained in the beginning of the chapter)of operation .

Mode 1 : In the first half cycle the capacitor 1 charges as the

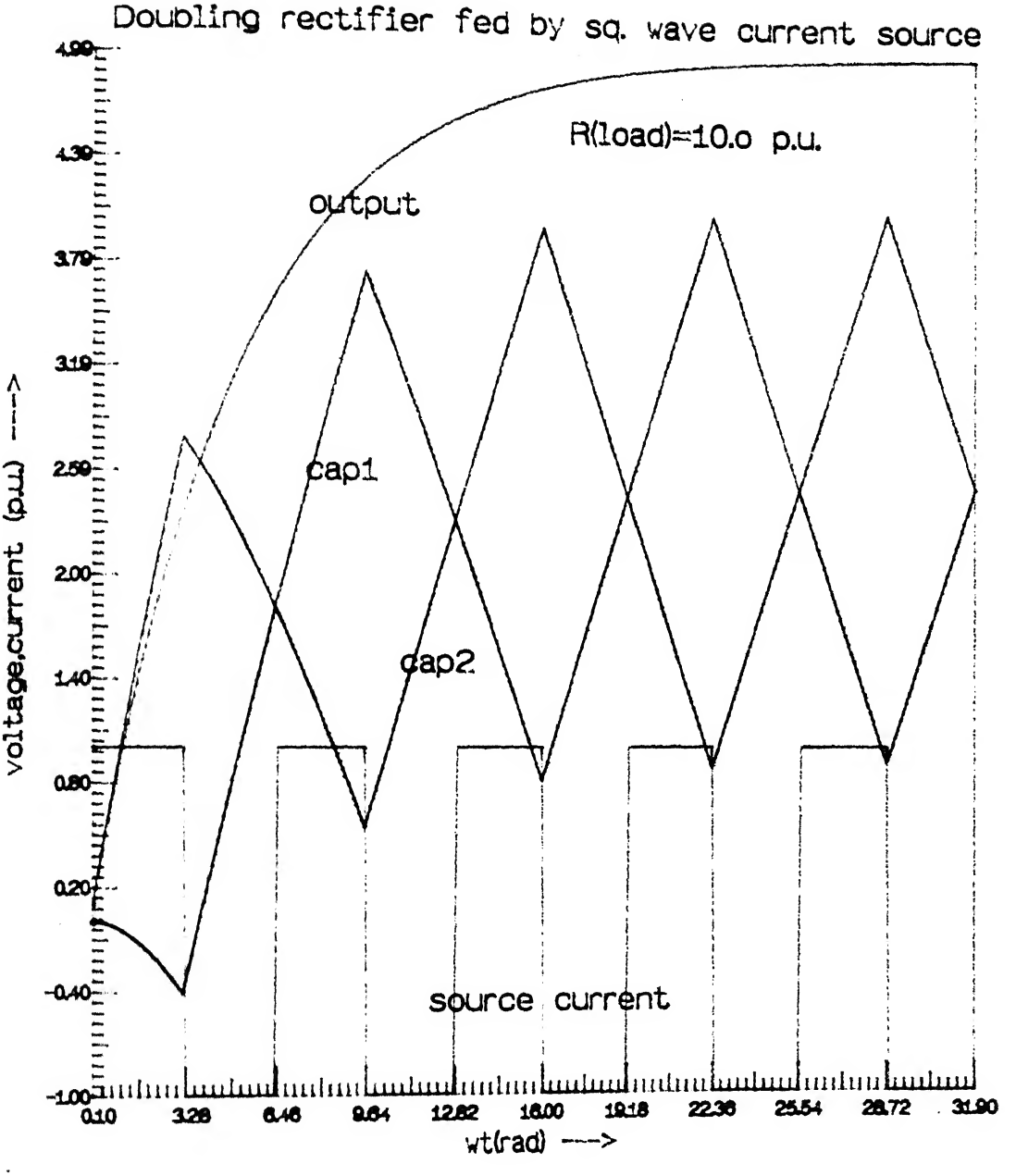


Fig.4.11 Loaded Transient and Steady State behaviour for the capacitor diode multiplier fed by square wave current source

supply current is positive . The capacitor 2 charges linearly in the negative direction . At the end of π radians ,the circuit transits to mode 2 owing to the fact that source current changes its direction .

Mode 2 : The capacitor 2 voltage starts rising from the negative value from where it was left when the circuit transited to mode 2. It becomes positive soon . The voltage across capacitor 1 falls linearly from where it was left at $\omega t = \pi$ when the circuit transited to mode 2 . This process of charging and discharging of capacitors 1 & 2 respectively in mode 1 and the reverse in mode 2 continues till the steady state is reached . In steady state the a.c. components of capacitors 1 & 2 voltages are 180^0 out of phase. Therefore the output voltage is nearly ripple free .The average ouput voltage is approximately 5.0 p.u.

OPERATION AS A CURRENT HALVER

From the average output voltage vs. load resistance characteristics of the rectifier , it is clear that the circuit works as a current halver. At a load resistance of 10.0 p.u., the average output voltage for the rectifier fed by sine wave and square wave current sources is 4.23 p.u. and 4.98 p.u. respectively. Hence the load current is 0.423 and 0.498 times the source current respectively. The results show that the load current is ,infact, lesser than half the input current for the rectifier fed by sine wave current source. This multiplication factor increases with the increase in load resistance and becomes 0.5 at a load resistance of about 1000.0 p.u. However, for the square wave current source the current halver operation is better

and is seen at very low values of load resistances too.

4.5.3 VARIATIONS IN AVERAGE OUTPUT VOLTAGE AND PEAK TO PEAK OUTPUT VOLTAGE RIPPLE WITH VARIATION IN LOAD RESISTANCE

4.5.3.1 *AVERAGE OUTPUT VOLTAGE vs. LOAD RESISTANCE*

The average output voltage increases as the load resistance is increased. It happens so because the source current is constant and any change in the output load resistance causes more current through capacitors. This enables them acquire more charge and as a result raise their voltages higher.In all this amounts to higher average output voltages.This is true for both the cases. Fig. 4.7 shows this behaviour.

4.5.3.2 *PEAK TO PEAK OUTPUT VOLTAGE RIPPLE vs. LOAD RESISTANCE*

Fig. 4.8 shows this behaviour.

(a) Square wave : The peak to peak output voltage ripple reduces as the load resistance is increased. The peak to peak output voltage ripple in square wave case is very low(zero for all practical purposes). This is due to the fact the ripples in voltages across capacitor 1 & 2 are out of phase by 180^0 and hence cancel each other.

(b) Sine wave : The ripple in the output voltage reduces as the load resistance is increased. This is due to the fact that at high values of load resistance, the variations in capacitors' voltages are small since the current through them is high as explained in sec. 4.5.3.1 above and the charge loss is minimal because of the high load resistance.

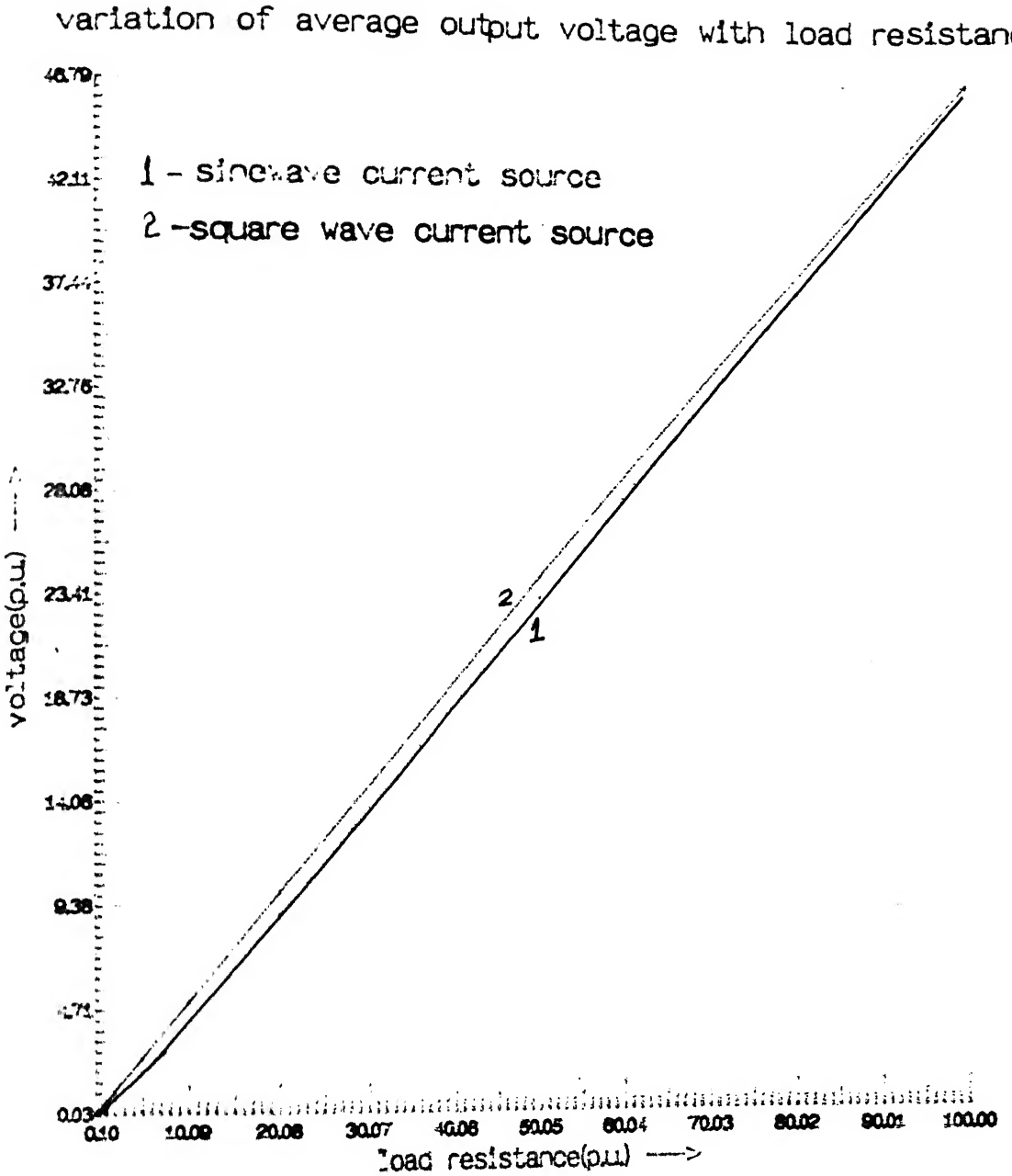
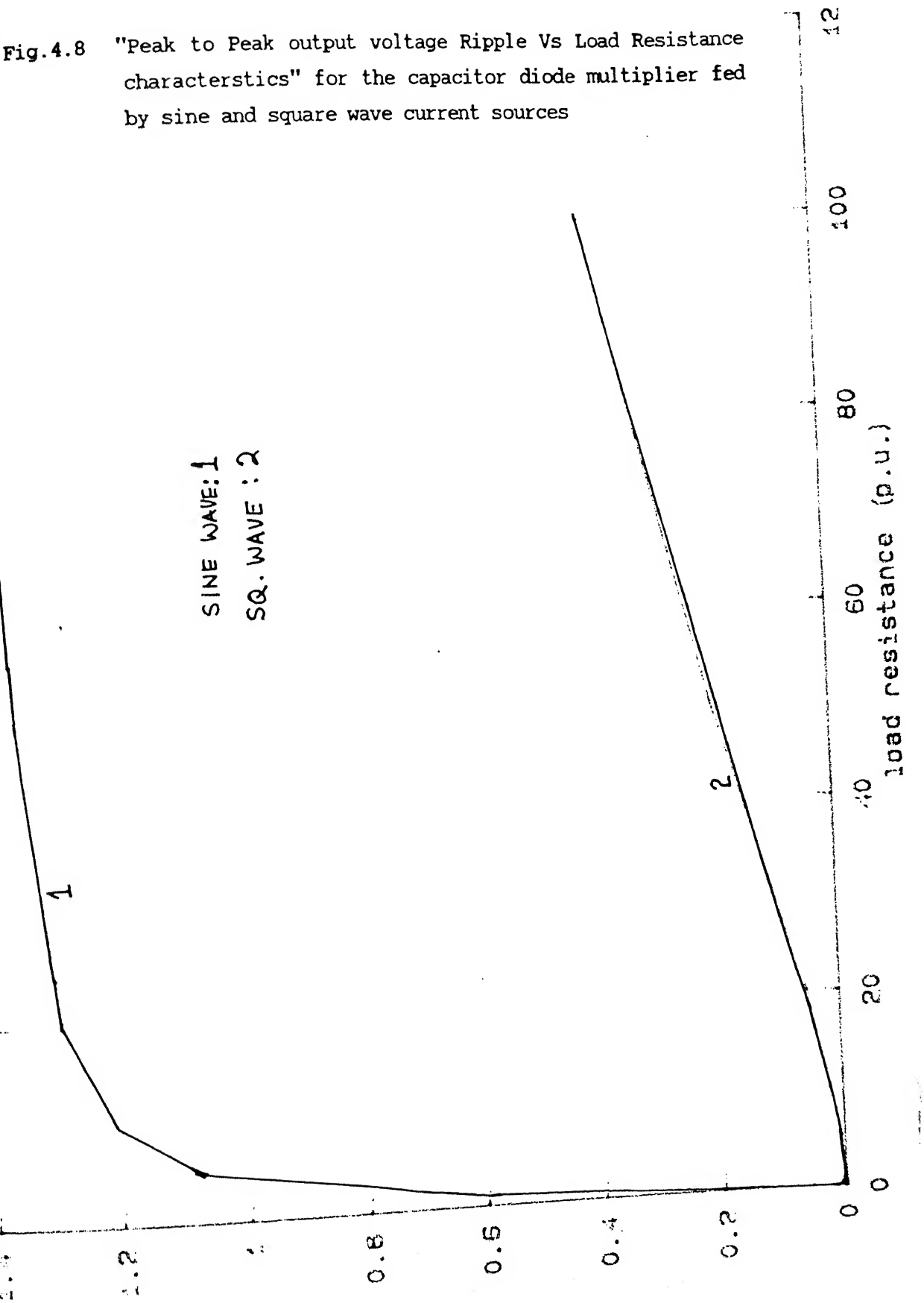


Fig.4.7 "Average output voltage Vs Load Resistance characterstics" for the capacitor diode multiplier fed by sine and square wave current source

Fig.4.8 "Peak to Peak output voltage Ripple Vs Load Resistance characterstics" for the capacitor diode multiplier fed by sine and square wave current sources



CHAPTER 5

SPICE SIMULATION

The circuit of Fig. 2.1 has been analysed in chapter 2 & chapter 3 for operation as a voltage doubling rectifier. This circuit can be modified to obtain an output voltage which is adjustable in the range of 0 to 2 p.u. These modifications are discussed in this chapter.

Need for controlling the output voltage arises in applications where regulation against variations in load and input supply is required. Some examples include HV power supplies for photomultiplier tubes used in scintillating counters, flying spot scanners etc.

5.1 METHODS OF CONTROLLING THE OUTPUT VOLTAGE

The voltage doubling rectifier of Fig. 2.1 can be modified in the following manners :

(1). The usual a.c. 50 hz input source can be replaced by an inverter operating from a fixed d.c. voltage source. This inverter can be modulated to obtain control of the output voltage. The control of the voltage rests in the inverter while the doubling rectifier is unaltered. This cnfiguration is shown in Fig. 5.1.

(2) An alternative is to modify the circuit of Fig.2.1 by replacing the diodes by switches. It is then possible to modulate the input voltage to control the d.c. output voltage. This

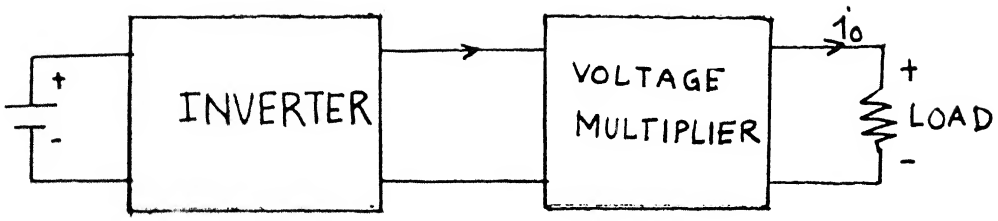


Fig.5.1 Voltage Multiplier fed by an Inverter operating on a fixed D.C source.

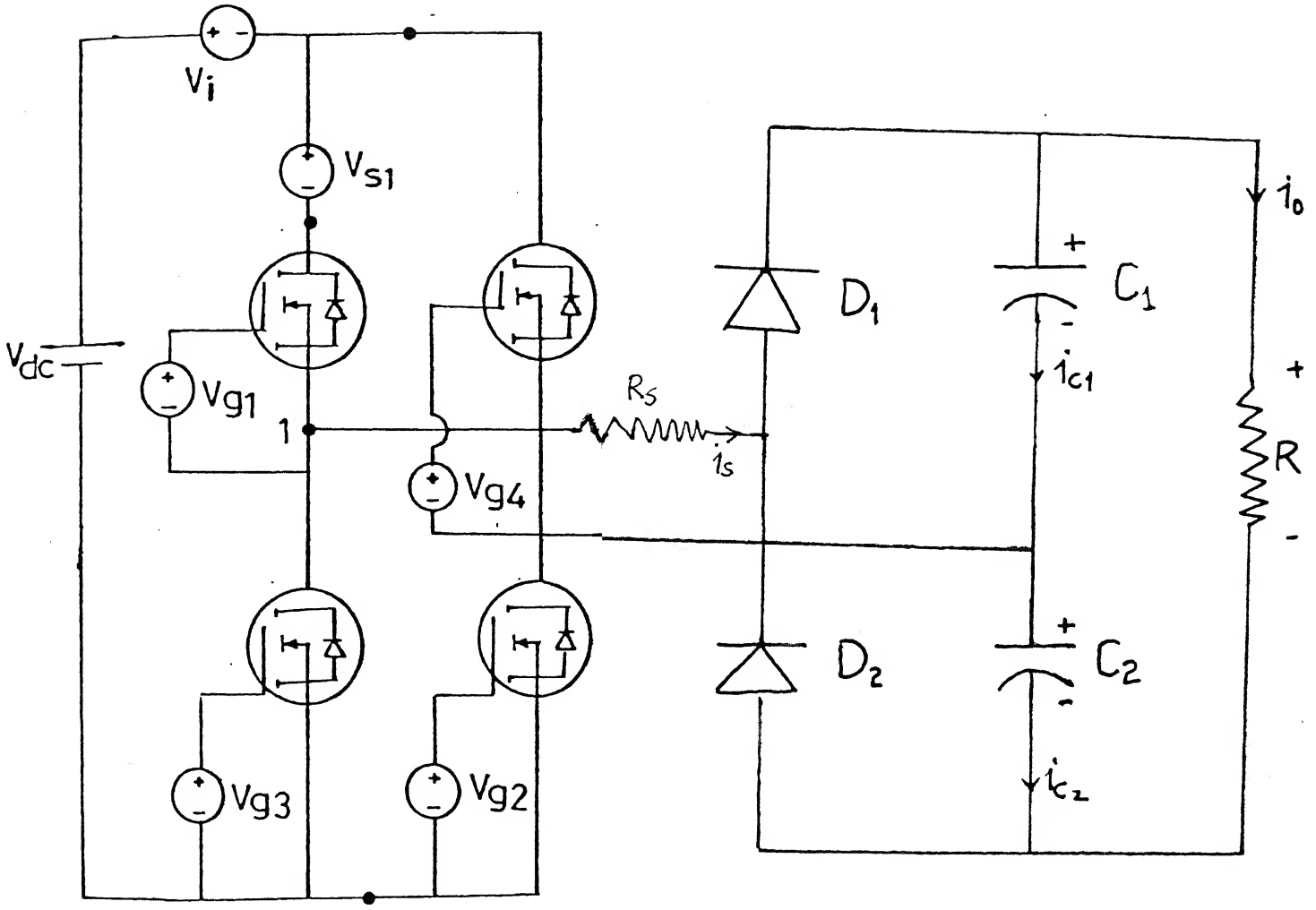


Fig.5.2 Voltage Doubling Rectifier fed by a Square wave Voltage source of controllable pulse width.

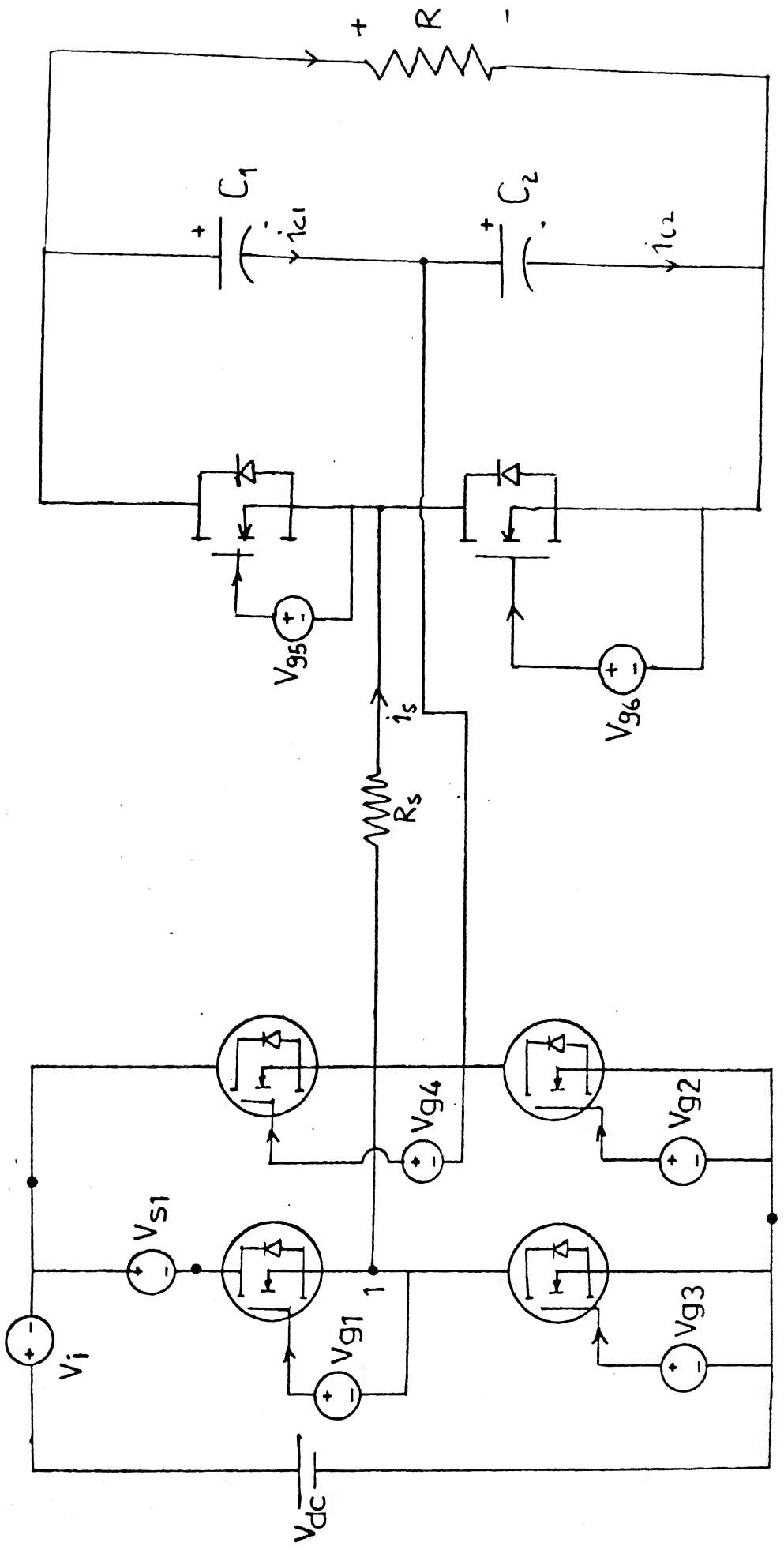


Fig.5.3 Modified Voltage Doubling Rectifier fed by an Inverter running at a constant frequency.

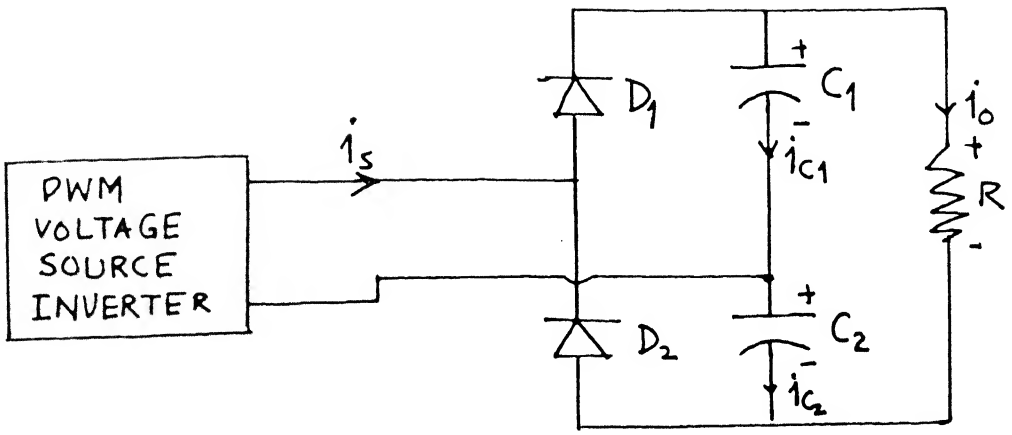


Fig.5.4 Voltage Doubling Rectifier fed by a PWM Voltage source.

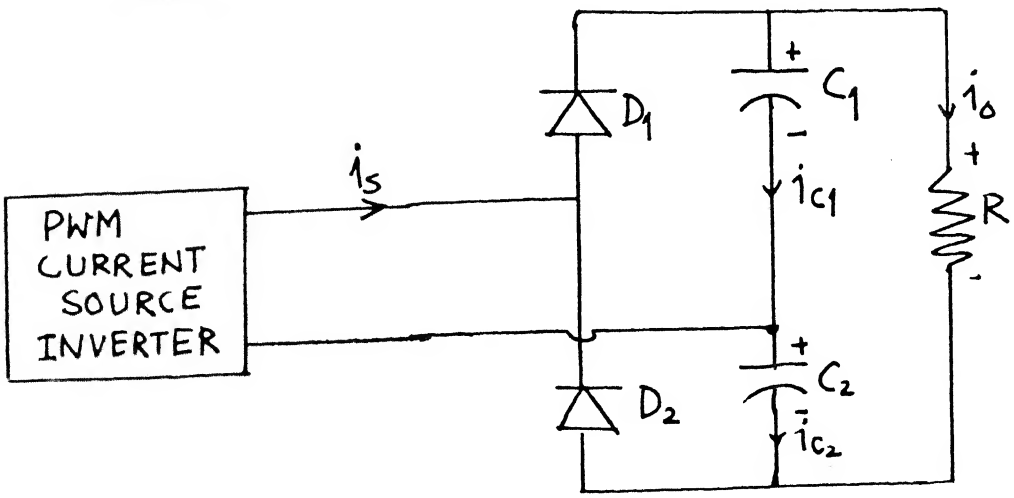


Fig.5.5 Voltage Doubling Rectifier fed by a PWM Current source.

.he input voltage to control the d.c. output voltage. This :onfiguration is shown in Fig.5.3. The square wave voltage is)ften conveniently generated by an inverter as shown in Fig.5.3 vhile in principle sine wave input can also be used. The problem)f reduced conduction due to charge on capacitors makes a square vave input preferable.

(3 The performance of capacitor - diode doubling rectifier fed by square wave and sine wave curent source has been given in chapter 4. The circuit configurations are given in Fig. 4.1(a) & (b). The input source can be modified to a Pulse Width Modulated current wave to obtain controlled output voltage as shown in Fig.5.4 & 5.5.

5.2 SIMULATION ON SPICE

The circuits (1) to (4) above have been simulated on SPICE version 3e2 available on main frame. SPICE is a computer aided circuit analysis program used for predicting the behaviour of electric and electronic circuits. Circuits are described to SPICE by use of an input file, which lists each circuit element(resistor, inductor, capacitance, voltage and/or current sources and semiconductor devices) and indicates how each is connected using node numbers. In addition there are lines in the input file which designate the frequency of the sources, temperature, the types of analyses to be done and how the results are to be presented. The program also has model lines which describe the model of the semiconductor devices being used.

The programs for the circuit of Fig. 5.1, 5.2, 5.3 and

isted in Appendix 3. The simulation of main subsystems in SPICE ıas been given below :

5.2.1 SIMULATION OF MOSFET INVERTER AND MODULATION IN IT

Enhancement mode NMOS is used as a switch in the full bridge inverter as shown in the Fig. 5.2. The MOSFET model chosen has the following details

Level (Model Index) = 1 (standard schichman hodges)

VTO (zero bias thresshold voltage) = 0

K_P (Transconductance Parameter) = 1

VTO and K_P define the d.c. characteristics of the device. The full bridge inverter consisting of 4 NMOS devices has four voltage sources connected as shown in fig. 5.2, one for each NMOS device, to switch on and off each NMOS. The switching of each NMOS is done in such a way as to generate square wave voltage of controllable pulse width. For switching on/off of the device, the square wave voltage source of the type given in sec. 5.2.2 is used.

5.2.2 SIMULATION OF THE PWM VOLTAGE SOURCE

PWM voltage source has been simulated by connecting six voltage sources in series. Three voltage sources give positive pulses in the positive half cycle and three voltage sources give negative pulses in the negative half cycle. The frequency of the voltage generated by each source is 50 hz. The voltage source is defined in the following manner

V_{in} = (V_1 V_2 T_d T_r T_f PW T_P)

V_{in} = square wave voltage source of

V_1 = voltage at $t = T_d^-$

V_2 = voltage at $t = T_d^+$

T_d = delay time

T_r = rise time

T_f = fall time

PW = pulse width (time during which voltage level is V_2)

T_p= Time period of the voltage source

The width in any of the voltage source can be varied to change the output voltage generated by the doubling rectifier.

5.2.3 SIMULATION OF THE PWM CURRENT SOURCE

PWM current source has been simulated by connecting six current sources in parallel. Three current sources give positive pulses in the positive half cycle and three current sources give negative pulses in the negative half cycle. The frequency of the current wave generated by each source is 50 hz. The current source is defined in the following manner

I_{in} = (I_1 I_2 T_d T_r T_f PW T_p)

where I_{in} = any periodic square wave current source of contollable width

I_1 = current at $t = T_d^-$

I_2 = current at $t = T_d^+$

T_d = delay time

T_r = rise time

T_f = fall time

level is I_2)

T_P= Time period of the current source

The width in any of the current source can be varied to change the output voltage generated by the capacitor diode multiplier.

5.3 SIMULATION AND PERFORMANCE OF THE CIRCUITS DESCRIBED IN SECTION 5.1

In this section the simulation of these controlled output voltage systems has been described. The following configurations have been studied.

(1) The configuration shown in Fig. 5.2 has been studied. The voltage source inverter has a single pulse of controlled width θ.

The pulse width can be modified in the range 0 to π to effect the change in the average output voltage and peak to peak output voltage ripple. The circuit of Fig. 5.2 with a load resistance of 500 ohms and capacitance of 100 μF was run. The performance of this circuit is given in the Fig.5.6(a) & (b). Some conclusions can be drawn from the simulation results:

At large values of the load resistance , the effect of change in the pulse width θ in the range from α to π, where α is very small, on the average output voltage is minimal. In other words, the output voltage is insensitive to the variations in the pulse width in this range. The output voltage, however, is sensitive to the variations in the pulse width in the range from 0 to α . The value of α is very low for large resistances. The smaller the resistance, higher will be the value of angle α. The value of α is

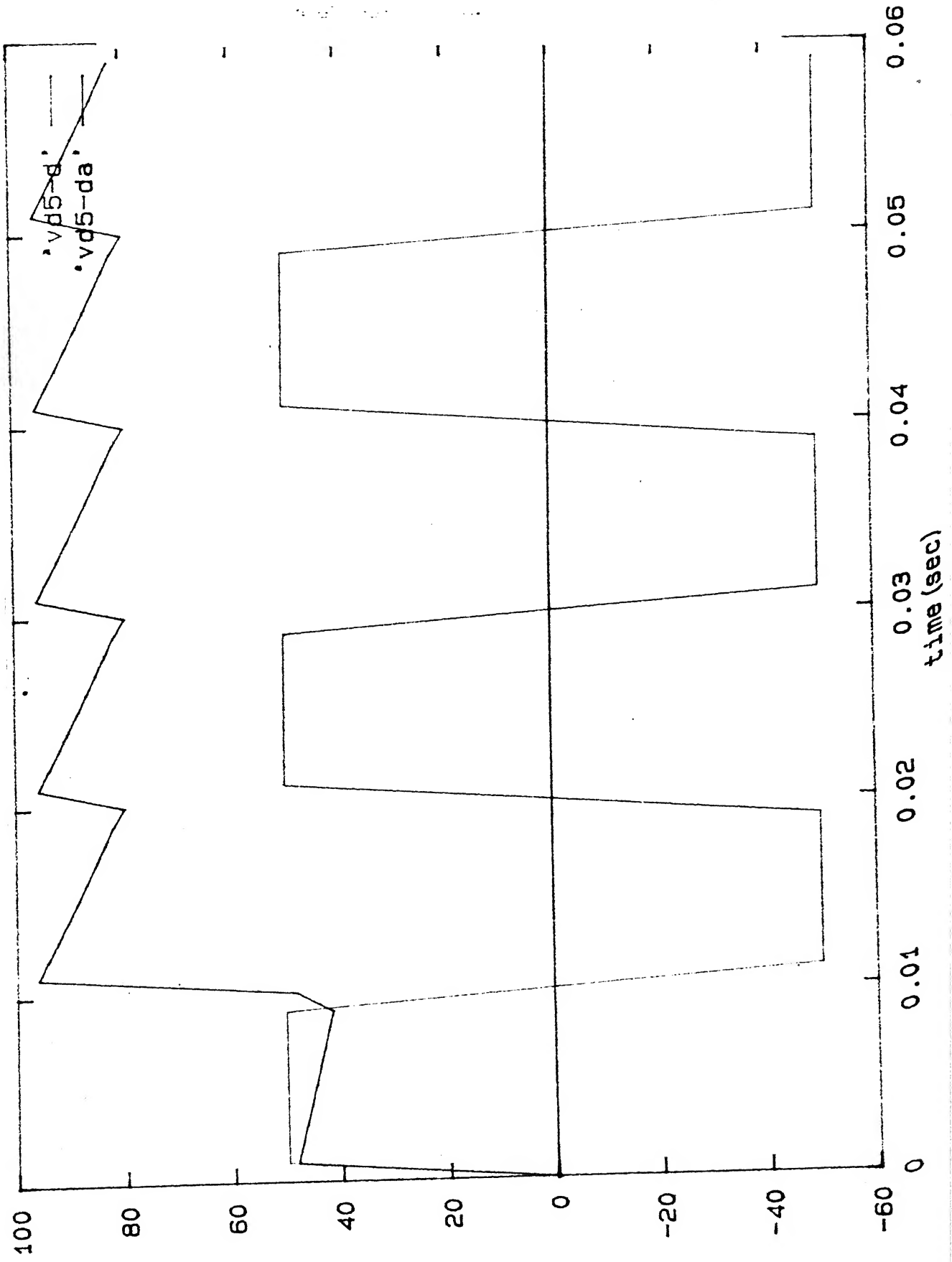
actually decided by the circuit elements R_s and Capacitor 1 or 2. If $R_s.C$ is coparable to the pulse width of the input square wave, charging and discharging of the capacitors 1 & 2 can be controlled and hence the average output voltage can be controlled. With the reduced pulse width, source current peaks are higher and hence the output voltage ripple as explained in the sec.3.1.4. The sensitivity of average output voltage to the variations in pulse width increases with the reduction in load resistance.This behaviour is clear from Fig. 4.6(b) where variation in average output voltage is plotted for two values of the load resistance.

(2) The performance of the doubling rectifier fed by a PWM voltage source with a load resistance of 1000 ohms and capacitance of 100μ has been studied and shown in Fig.5.8. The PWM scheme uses 3 pulses /180 degrees and the frequency is fixed at 50 hz. The generation of PWM voltage source using SPICE3 has been discussed in sec. 5.2.

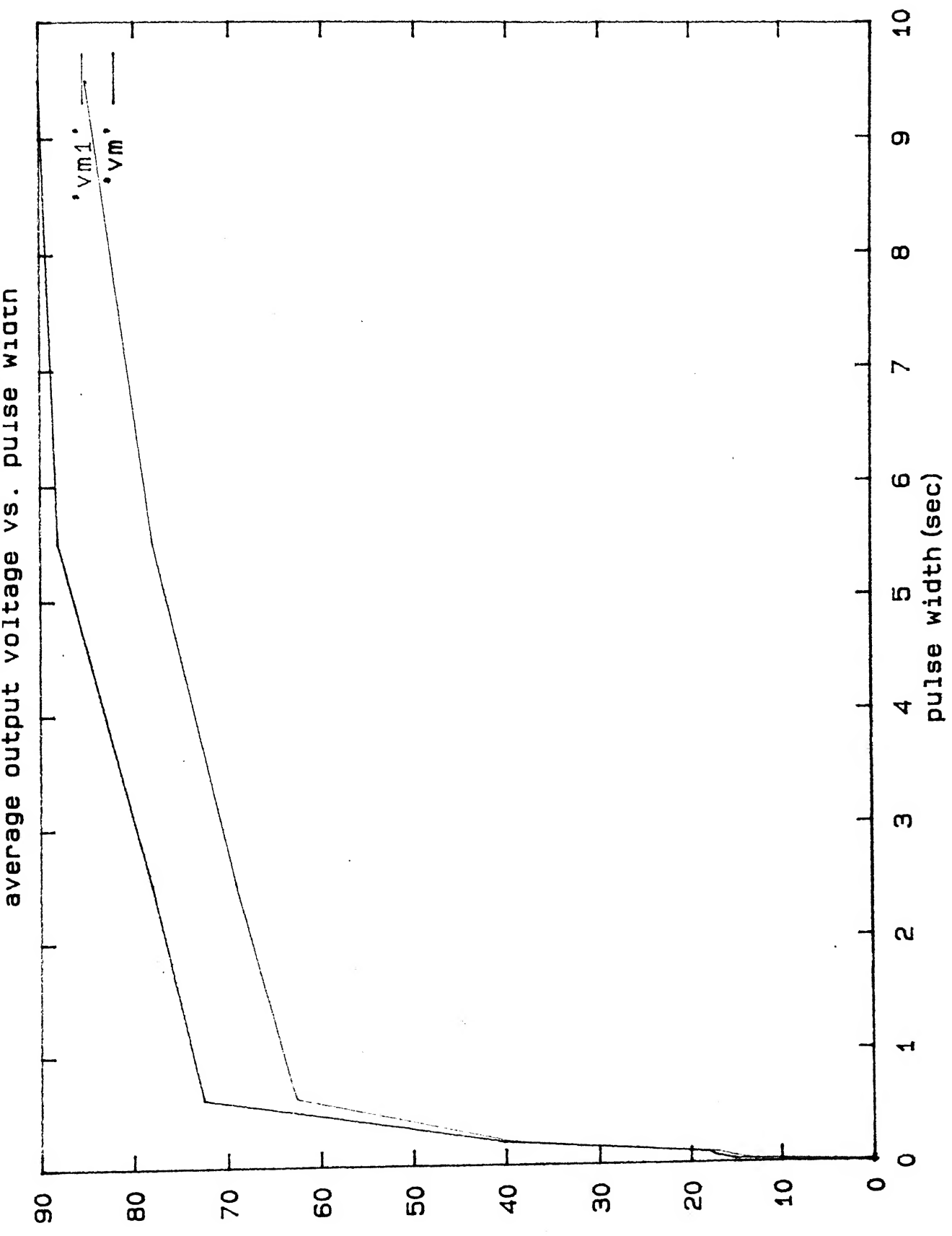
(3) The configuration shown in Fig.5.3 with a load resistance of 5000 ohms and capacitance of 25.5μF was simulated. The MOS inverter is running at 25 hz . The switches inside the multiplier were used to generate a controllable single pulse in each half cycle. The simulation of MOS inverter using SPICE3 is given in the section 5.2. Performance is given in Fig.5.7.

(4) The configuration shown in Fig.5.5 with a load resistance of 120 ohms and capacitance of 200μF was simulated. The PWM current source has three pulses in 180 degrees and is operating at 50 hz.

Fig.5.6(a) Behaviour of the circuit of Fig.5.2



the Square Wave voltage.



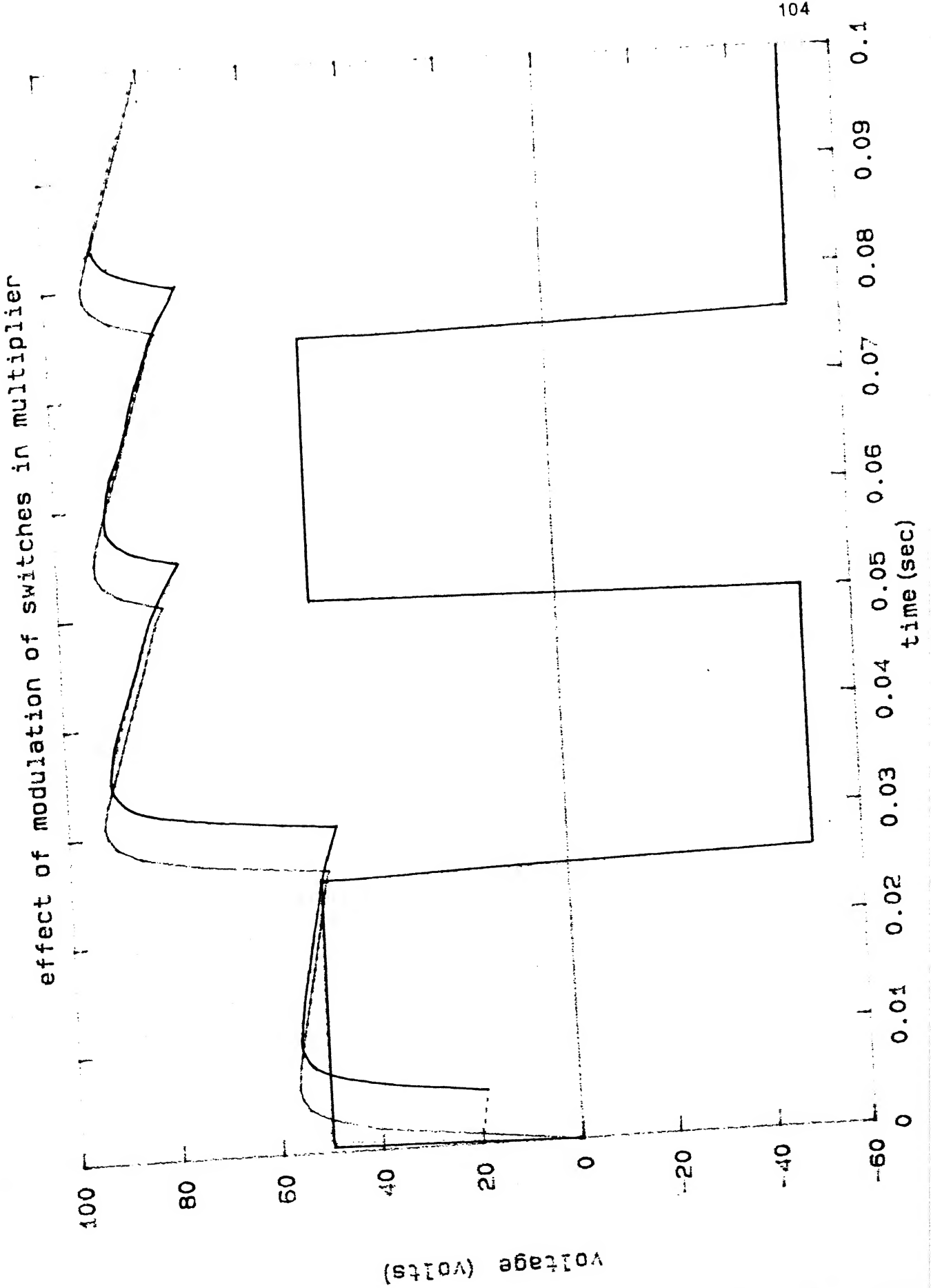
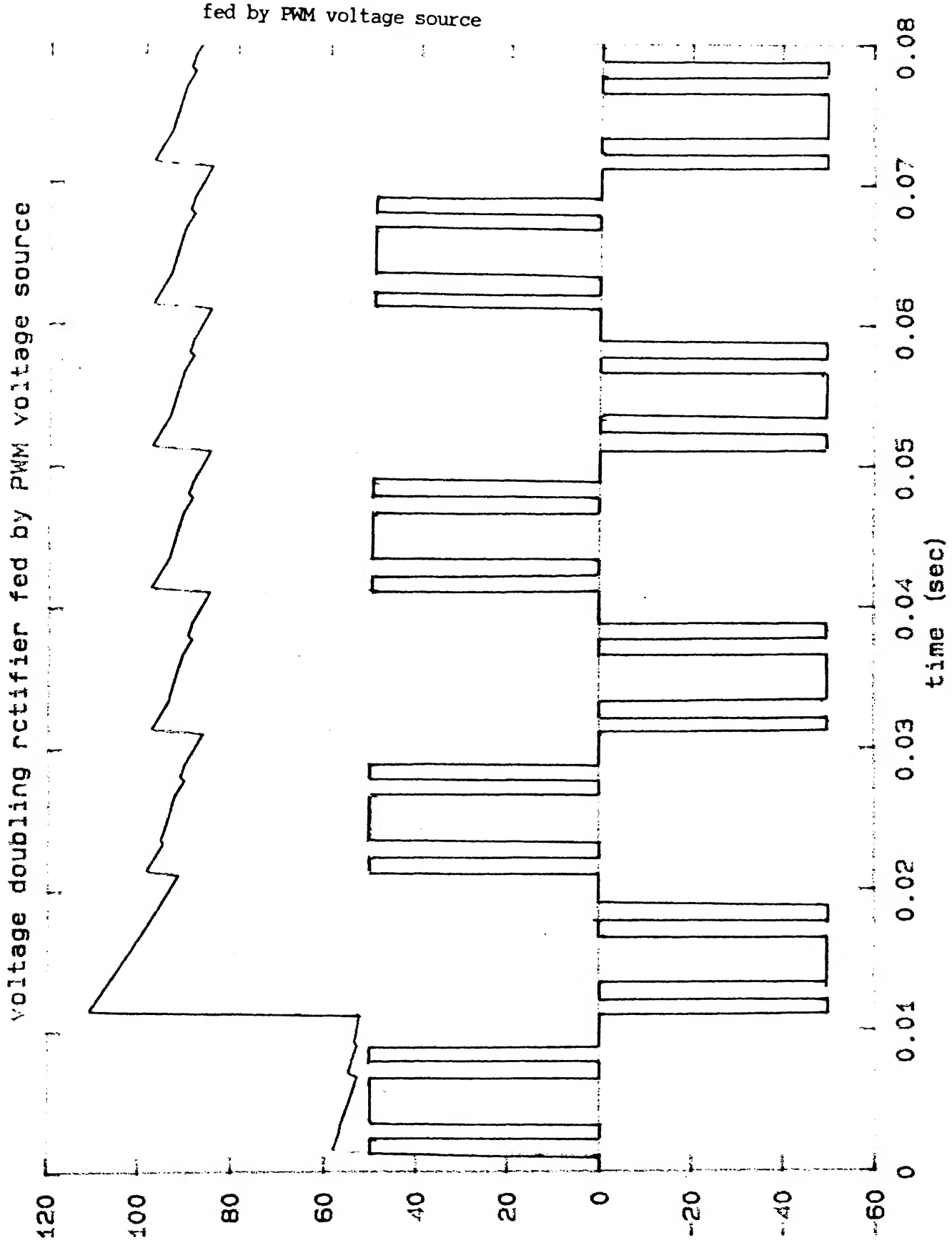


Fig.5.7 Behavior of the Modified Voltage Doubling Rectifier fed by an Inver

Fig.5.8 Behavior of the circuit of voltage doubling rectifier fed by PWM voltage source



Performance is given in Fig.5.9. The average output voltage can be better controlled in this scheme as the voltage build up across the capacitors is directly proportional to the charge supplied to them. By controlling the width of the pulses, we can control the voltage rise and fall across capacitors and hence the average output voltage.The simulation of PWM current source has been given in the sec.5.2.

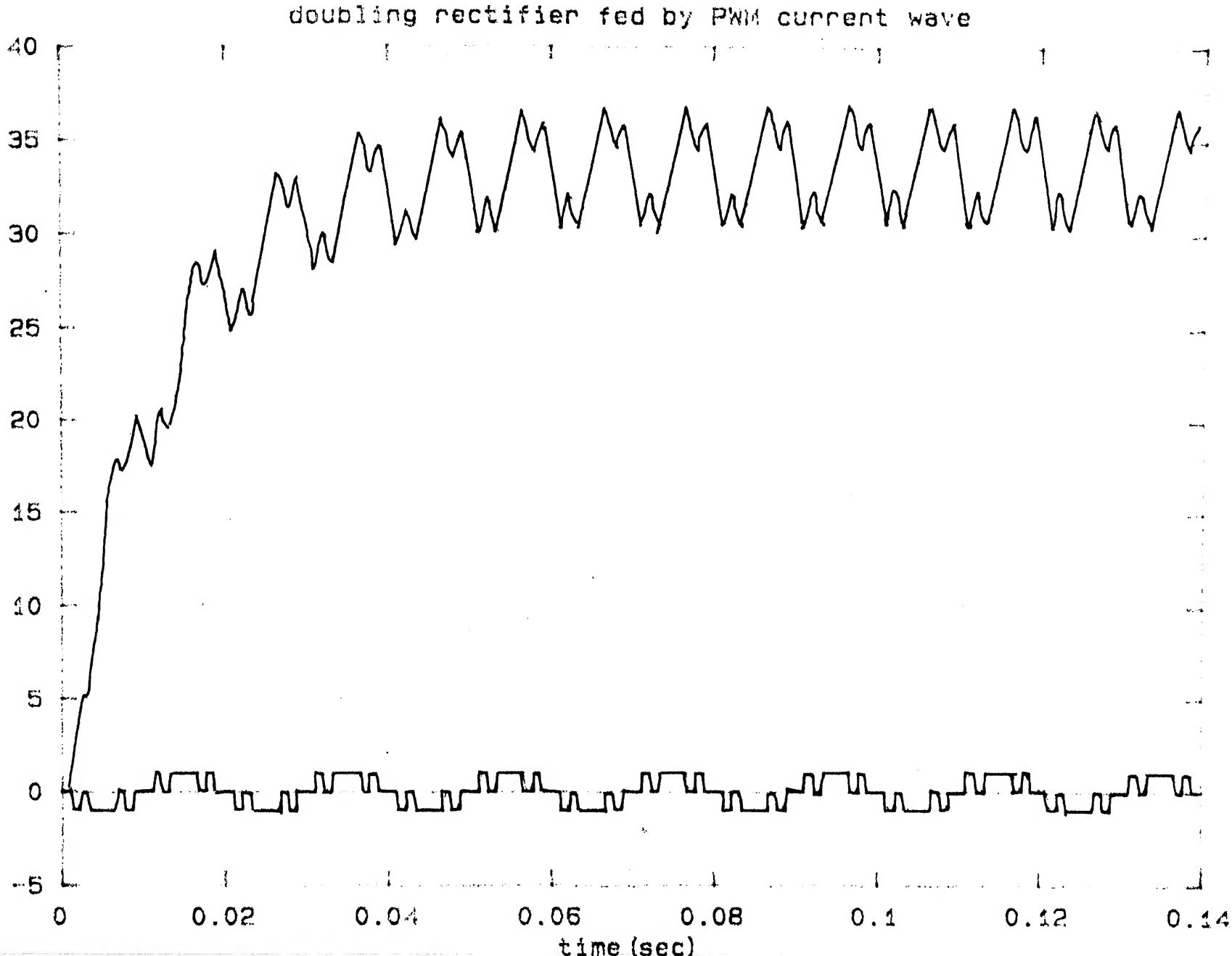


Fig.5.9 Behavior of the circuit of voltage doubling rectifier

CONCLUSIONS

Based upon the analysis and simulation carried out in this thesis, the following conclusions can be drawn:

(1) The full wave voltage doubling rectifier fed by an ideal sine wave voltage source has been analysed and simulated. Simulation results show that the circuit works as an acceptable voltage doubling rectifier(average output voltage >1.9p.u.) for the values of load resistances greater than approximately 100.0 p.u. The performance degrades fast as the load resistance is reduced below 100.0 p.u. Peak to peak output voltage ripple increases with the reduction in load resistance.

(2) The full wave doubling rectifier fed by a square wave voltage source has been analysed and simulated. Simulation results show that its performance is better in terms of the output voltage regulation and peak to peak output voltage ripple as compared to the doubling rectifier in (1) above. However, the source curent peaks are much higher in this case. e. Diodes are found to conduct impulse of currents at $\omega t = 0, \pi, 2\pi$.. .

3 (a) The voltage doubling rectifier fed by nonideal sine wave and square wave voltage sources has been analysed and simulated. The simulation results show that on a particualar value of ωLs, the average output voltage is maximum.The voltage

falls as we increase the value of ωLs above it or reduce the value of ωLs below it. This is found to be true for both nonideal sine and square wave voltage sources.

(b) The effect of ωLs on peak to peak output voltage ripple is different in the two systems.For the rectifier fed by nonideal sine wave voltage source, the peak to peak output voltage rippple increases as the source reactance is increased. For the rectifier fed by non ideal square wave voltage source, the peak to peak output voltage ripple decreases as the source reactance is increased.

(c) The variation in peak to peak output voltage ripple for the doubling rectifier fed by non ideal sine wave voltage source is quite complex. For low values of ωLs (<0.04 p.u.), the increse in load resistance reduces the peak to peak output voltage ripple. For values of ωLs larger than 0.04 p.u.,the increase in load resistance till a particular value reduces the peak to peak output voltage ripple and a further increase in the value of load resistance beyond this value causes an increase in the output voltage ripple.

Same thing is true for the variation in average output voltage with variations in load resistance .i.e.,average output voltage increases with increase in load resistance initially till a particular value of load resistance. If the load resistance is increased further, the output voltage falls..

For the rectifier fed by a non ideal square wave voltage source, it is simpler to understand the behaviour of ripple voltage against variations in load resistance. The peak to peak output voltage ripple reduces with the increase in the load

resistance.

(4) The transient behaviour of the doubling rectifier fed the two voltage sources is also different. The rectifier fed by non ideal square wave voltage source shows the phenomenon of multiple conduction of diodes D_1 and D_2 in positive and negative half cycles respectively. The doubling rectifier fed by sine wave voltage source ,however , does not show any such phenomenon.

(5) The frequency of the ripple in the output voltage keeps on reducing as the load resistance is increased. For the Values of R_L lesser than 30.61 p.u. , the output voltage ripple frequency is twice as that of the supply frequency. This phenomenon is not observed in the rectifier fed by non ideal square wave voltage source.

(6) The doubling rectifier fed by square and sine wave current sources has been analysed and simulated. The simulation results show that both the circuits work as a current halver.

Voltage multiplier fed by sine wave current sources takes a large no. of cycles in reaching the steady state . However , the multiplier fed by square wave voltage source has a very small transient period.

(7)Some methods to control the output voltage have been suggested and simulated on SPICE. The doubling rectifier fed by a square wave voltage source of controllable pulse width shows that

for large values of load resistance, the average output voltage is not much sensitive to the modulation of pulse width. The average output voltage does not change much in the range of the pulse width from α to π where α is small and depends upon the product of R_s, the equivalent source resistance, and the capacitance, C. However, in the range of the pulse width from 0 to α, the output voltage is very much sensitive to change in pulse width.

As the load resistance is reduced the sensitivity of output voltage to the variations in pulse width increases. Output voltage ripple increases as the pulse width is reduced in the pulse width range of 0 to 180 degrees.

Modified voltage doubling rectifier and the rectifier fed by PWM voltage source also show the similar behaviour as explained above. The PWM current source gives much better control.

SUGGESTIONS FOR THE FUTURE WORK

(1) Mathematical analysis of the doubling rectifier fed by a square wave voltage source of controllable pulse width can be done and expressions obtained for calculating the output voltage regulation and percentage ripple.

(2) A better method of controlling the voltage douling rectifier has to be worked out for low values of load resistance. Detailed analysis of the effect of PWM voltage and current sources can be done.

APPENDIX NO. 1

Derivations of the expressions for $VC_2(\alpha)$, $VC_2(\beta)$ and $VC_1(\pi+\alpha)$ are given here. Equations 2.2, 2.5, 2.6, 2.11, 2.12, 2.16, 2.19 and 2.20 are required for above derivations and hence are being reproduced here.

In Mode 1 from $\omega t = \alpha$ to $\omega t = \beta$, we have

$$VC_1 = E_m \text{ Sin } \omega t \qquad 2.2$$

$$VC_2 = \frac{-E_m}{1+\omega^2R^2C^2} \text{ Sin } \omega t + K_1 \exp(-t/RC) + \frac{E_m \omega RC}{1+\omega^2R^2C^2} \cos \omega t \qquad 2.5$$

$$K_1 = \left\{VC_2(\alpha) + \frac{E_m \sin(\alpha)}{1+\omega^2R^2C^2} - \frac{E_m \omega RC \cos(\alpha)}{1+\omega^2R^2C^2}\right\} \exp\left[\frac{\alpha}{\omega RC}\right] \qquad 2.6$$

Let $l_1 = \dfrac{E_m}{1+\omega^2R^2C^2}$ and $l_2 = \dfrac{E_m \omega RC}{1+\omega^2R^2C^2}$, then

$$VC_2 = - l_1 \sin \omega t + K_1 \exp(-t/RC) + l_2 \cos \omega t \qquad 2.5a$$

$$K_1 = [VC_2(\alpha) + l_1 \sin(\alpha) - l_2 \cos(\alpha)] \qquad 2.6a$$

In Mode 2 from $\omega t = \beta$ to $\pi+\alpha$, we have

$$VC_1 = E_m \sin(\beta) \exp\left[\frac{-2}{RC\omega} (\omega t-\beta)\right] \qquad 2.11$$

$$VC_2 = VC_2(\beta) \exp\left[\frac{-2}{RC\omega} (\omega t-\beta)\right] \qquad 2.12$$

In mode 3 from $\omega t = \alpha+\pi$ to $\beta+\pi$, we have

$$VC_2 = - E_m \sin \omega t \qquad 2.16$$

$$VC_1 = I_1[\sin \omega t - \omega^2 R^2 C^2 \cos \omega t] + K_2 \exp(-t/RC) \qquad 2.19$$

$$K_2 = VC_1(\pi+\alpha) + I_1[\sin(\alpha) - \omega^2 R^2 C^2 \cos(\alpha)] \exp\left(\frac{\pi+\alpha}{\omega^2 R^2 C^2}\right) \qquad 2.20$$

In mode 2 again from $\omega t = \pi+\beta$ to $2\pi + \alpha$, we have

$$VC_1 = VC_1(\pi+\beta) \exp\left[\frac{-2}{RC\omega} (\omega t - (\pi+\beta))\right] \qquad 2.50$$

$$VC_2 = Em \sin(\beta) \exp\left[\frac{-2}{RC\omega} (\omega t - (\pi+\beta))\right] \qquad 2.51$$

From 2.51, we have

$$VC_2(2\pi+\alpha) = Em \sin(\beta) \exp\left[\frac{-2}{RC\omega} (\pi+\alpha-\beta)\right]$$
$$= VC_2(\alpha) \qquad 2.52$$

From 2.12, we have

$$VC_2(\alpha+\beta) = VC_2(\beta) \exp\left[\frac{-2}{RC\omega} (\pi+\alpha-\beta)\right] \qquad 2.53$$

From 2.16,

$$VC_2(\alpha+\pi) = E_m \sin(\alpha) \qquad 2.54$$

Hence

$$VC_2(\beta) = E_m \sin(\alpha) \exp\left[\frac{2}{RC\omega} (\pi+\alpha+\beta)\right] \qquad 2.55$$

From Eq. 2.11

$$VC_1(\pi+\alpha) = Em \sin(\beta) \exp\left[\frac{-2}{RC\omega} (\pi+\alpha-\beta)\right] \qquad 2.56$$

Equation 2,52, 2.55 and 2.56 give the expressions for $VC_2(\alpha)$, $VC_2(\beta)$ and $VC_1(\pi+\alpha)$ respectively.

D02BAF – NAG FORTRAN Library Routine Document

NOTE before using this routine, please read the appropriate implementation document to check the interpretation of ***bold italicised*** terms and other implementation-dependent details. The routine name may be precision-dependent.

1. Purpose

D02BAF integrates a system of first-order ordinary differential equations over a range with suitable initial conditions, using a Runge–Kutta–Merson method.

2. Specification

```
      SUBROUTINE D02BAF (X, XEND, N, Y, TOL, FCN, W, IFAIL)
C     INTEGER N, IFAIL
C     real X, XEND, Y(N), TOL, W(N,7)
C     EXTERNAL FCN
```

---

3. Description

The routine integrates a system of ordinary differential equations

$$Y_i' = F_i(T,Y_1,Y_2,...,Y_N), \qquad i = 1,2,...N,$$

from T = X to T = XEND using a Merson form of the Runge–Kutta method. The system is defined by a subroutine FCN supplied by the user, which evaluates F_i in terms of T and $Y_1,Y_2,...,Y_N$ (see Section 5), and the values of $Y_1,Y_2,...,Y_N$ must be given at T = X.

The accuracy of the integration is controlled by the parameter TOL.

For a description of Runge–Kutta methods and their practical implementation see [1].

4. References

[1] HALL, G. and WATT, J.M. (eds).
Modern Numerical Methods for Ordinary Differential Equations, p. 59.
Clarendon Press, Oxford, 1976.

5. Parameters

X – ***real.***

Before entry, X must be set to the initial value of the independent variable T.

On exit, it contains XEND, unless an error has occurred, when it contains the value of T at the error.

XEND – ***real.***

On entry, XEND must specify the final value of the independent variable. If XEND < X on entry, integration will proceed in the negative direction.

Unchanged on exit.

N – INTEGER.

On entry, N must specify the number of differential equations.

Unchanged on exit.

Y – ***real*** array of DIMENSION at least (N).

Before entry, Y(1),Y(2),...,Y(N) must contain the initial values of the solution $Y_1,Y_2,...,Y_N$.

On exit, Y(1),Y(2),...,Y(N) contain the computed values of the solution at the final value of T.

TOL – ***real.***

Before entry, TOL must be set to a **positive** tolerance for controlling the error in the integration.

The routine D02BAF has been designed so that for most problems a reduction in TOL leads to an approximately proportional reduction in the error in the solution at XEND. However, the actual relation between TOL and the accuracy achieved cannot be guaranteed. The user is strongly recommended to call D02BAF with more than one value for TOL and to compare the results obtained to estimate their accuracy. In the absence of any prior knowledge, the user might compare the results obtained by calling D02BAF with $TOL = 10.0^{-P}$ and $TOL = 10.0^{-P-1}$ if P correct decimal digits in the solution are required.

TOL is normally unchanged on exit. However, if the range X to XEND is so short that a small change in TOL is unlikely to make any change in the computed solution then, on return, TOL has its sign changed. This should be treated as a warning that the computed solution is likely to be more accurate than would be produced by using the same value of TOL on a longer range.

FCN – SUBROUTINE, supplied by the user.

FCN must evaluate the functions F_i (i.e. the derivatives Y_i') for given values of its arguments $T, Y_1, ..., Y_N$.

Its specification is:

```
SUBROUTINE FCN(T,Y,F)
real T,Y(n),F(n)
```

where n is the actual value of N in the call of D02BAF.

T – *real*.

On entry, T specifies the value of the argument T.

Its value must not be changed.

Y – *real* array of DIMENSION (n).

On entry, Y(I) contains the value of the argument Y_I, for I = 1,2,...,n.

These values must not be changed.

F – *real* array of DIMENSION (n).

On exit, F(I) must contain the value of F_I, I = 1,2,...,n.

FCN must be declared as EXTERNAL in the (sub)program from which D02BAF is called.

W – *real* array of DIMENSION (N,p), where $p \geq 7$.

Used as working space.

IFAIL – INTEGER.

On entry, IFAIL must be set to 0 or 1. For users not familiar with this parameter (described in Chapter P01) the recommended value is 0.

Unless the routine detects an error (see next section), IFAIL contains 0 on exit.

6. Error Indicators and Warnings

Errors detected by the routine:–

IFAIL = 1

On entry, TOL $\leq$ 0.0
or N $\leq$ 0.

(The latter error will cause a program breakdown with some compilers.)

IFAIL = 2

With the given value of TOL, no further progress can be made across the integration range from the current point T = X, or the dependence of the error on TOL would be lost if further progress across the integration range were attempted (see Section 11 for a discussion of this error exit). The components Y(1),Y(2),...,Y(N) contain the computed values of the solution for the current point T = X.

IFAIL = 3

TOL is too small for the routine to start the integration (see Section 11). X and Y(1),Y(2),...,Y(N) retain their initial values.

IFAIL = 4

A serious error has occurred in an internal call to D02PAF. Check all subroutine calls and array dimensions. Seek expert help.

7. Auxiliary Routines

Details are distributed to sites in machine-readable form.

8. Timing

This depends on the complexity and mathematical properties of the system of differential equations defined by FCN, on the length of the range and on the tolerance. There is also a small overhead of the form A + B × N, where A and B are machine-dependent computing times.

9. Storage

The storage required by internally declared arrays including those of auxiliary routines, is 28 *real* elements.

10. Accuracy

The accuracy depends on TOL, on the mathematical properties of the differential system, on the length of the range of integration and on the method. It can be controlled by varying TOL but the approximate proportionality of the error to TOL holds only for a restricted range of values of TOL. For TOL too large, the underlying theory may break down and the result of varying TOL may be unpredictable. For TOL too small, rounding errors may affect the solution significantly and an error exit with IFAIL = 2 or IFAIL = 3 is possible.

The user who requires a more reliable estimate of the accuracy achieved than can be obtained by varying TOL, is recommended to call the routine D02BDF where both the solution and a global error estimate are computed.

11. Further Comments

If the routine fails with IFAIL = 3, then it could be called again with a larger value of TOL (if this has not already been tried). If the accuracy requested is needed and cannot be obtained with this routine then the system may be very stiff (see below) or so badly scaled that it cannot be solved to the required accuracy.

If the routine fails with IFAIL = 2, it is probable that it has been called with a value of TOL which is so small that a solution cannot be obtained on the range X to XEND. This can happen for well-behaved systems and very small values of TOL. The user should, however, consider whether there is a more fundamental difficulty. For example,

(i) in the region of a singularity (infinite value) of the solution, the routine will usually stop with IFAIL = 2, unless overflow occurs first. If overflow occurs using D02BAF, routine D02PAF can be used instead to trap the increasing solution before overflow occurs. In any case, numerical integration cannot be continued through a singularity, and analytical treatment should be considered.

(ii) for 'stiff' equations, where the solution contains rapidly decaying components, the routine will use very small steps in T (internally to D02BAF) to preserve stability. This will exhibit itself by making the computing time excessively long, or occasionally by an exit with IFAIL = 2. Merson's method is not efficient in such cases, and the user should try the Gear method D02EAF.

To determine whether a problem is stiff, the routine D02BDF may be used.

Users with problems for which D02BAF is not sufficiently general should consider the routines D02BBF, D02BHF or D02PAF. Routine D02BBF can be used when output is required at points outside the range X to XEND (for example, for graph-plotting purposes) or more general error control is required. Use of D02BBF should be computationally more efficient than repeated calls to D02BAF to achieve the same result. Routine D02BHF can be used to calculate where a function of the components $Y_1, Y_2, \ldots, Y_N$ and their derivatives take a specified value.

D02PAF is a more general Merson routine with many facilities including more general error control options and several criteria for interrupting the calculations.

12. Keywords

Initial Value Problems,
Ordinary Differential Equations,
Runge–Kutta–Merson Method.

PROGRAM NO. 1

```
voltage doubler fed from a mos inverter
vin 1 0 dc 50
vin1 2 3 pulse(-2 10 0m 0.1m 0.1m 10m 20m)
vin2 4 5 pulse(-2 10 10m 0.1m 0.1m 10m 20m)
vin3 7 0 pulse(-2 10 0m 0.1m 0.1m 10m 20m)
vin4 6 0 pulse(-2 10 10m 0.1m 0.1m 10m 20m)
mos1 1 2 3 3 simple
mos2 1 4 5 5 simple
mos3 3 6 0 0 simple
mos4 5 7 0 0 simple
rs 3 9 1
d1 9 10 d
d2 11 9 d
c1 10 5 100u
c2 5 11 100u
r1 10 11 1000
*re 5 11 100meg
*re1 11 0 200meg
*re2 4 0 700meg
*re3 3 0 200meg
*re10 10 0 200meg
.options nopage
.model simple nmos(kp=1,vto=1,level=1)
.model d d
.tran 1m 60m
.plot tran v(10,11)
.end
```

PROGRAM NO. 2

```
voltage doubling rectifier fed by mos inverter
*diodes in the doubling rectifier replaced by switches
vin 10 0 dc 50
vin1 20 9 pulse(-2 10 0 0.02m 0.02m 25m 50m)
vin2 14 0 pulse(-2 10 25m 0.02m 0.02m 25m 50m)
```

```
vin4 15 0 pulse(-2 10 0 0.02m 0.02m 25m 50m)
vg1 2 3 pulse(-2 10 5m 0.02m 0.02m 20m 50m)
vg2 6 1 pulse(-2 10 30m 0.02m 0.02m 20m 50m)
*mosfet switches
mos1 10 12 9 9 simple
mos2 9 14 0 0 simple
mos3 10 13 7 7 simple
mos4 7 15 0 0 simple
m2 5 6 1 1 simple
m1 1 2 3 3 simple
c1 4 7 25.5u
*reverse recovery diodes
da 19 13 d1
db 20 12 d1
dp 9 10 d1
dq 7 10 d1
dr 0 9 d1
ds 0 7 d1
rs1 9 1 5
r1 4 11 5000
c2 7 11 25.5u
*mega ohm resistors provided
*so that each node
*gets a DC path to ground
re1 7 11 100meg
re2 9 0 100meg
re3 7 0 100meg
re4 1 0 100meg
re5 3 0 100meg
re6 5 0 100meg
re7 12 0 100meg
re8 19 0 900meg
d1 11 5 d1
d2 3 4 d1
.tran 1m 100m uic
```

```
.model simple nmos(vto=1,kp=1,level=1)
.model dl d
.options nopage
.plot tran v(4,11)
.plot tran v(9,7)
.end
```

PROGRAM NO. 3

```
voltage doubler PWM ANALYSIS
* definition of a PWM voltage source
vin1 1 2 pulse(0 50 1.11m 0.01m 0.01m 1.11m 20m)
vin2 2 3 pulse(0 50 3.33m 0.01m 0.01m 3.33m 20m)
vin3 3 4 pulse(0 50 7.77m 0.01m 0.01m 1.11m 20m)
vin4 4 5 pulse(0 -50 11.11m 0.01m 0.01m 1.11m 20m)
vin5 5 6 pulse(0 -50 13.33m 0.01m 0.01m 3.33m 20m)
vin6 6 0 pulse(0 -50 17.77m 0.01m 0.01m 1.11m 20m)
*source resistance
rs 1 8 1
*diodes and capacitances
dl 8 9 dl
cl 9 0 100u
c2 0 10 100u
d2 10 8 dl
*load resistance
rl 9 10 1000
*default model of the diode
.model dl d
.options nopage
*transient analysis
.tran 0.1ms 80ms
*plot output voltage and input voltage
.plot tran v(9,10)
.plot tran v(1)
.end
```

PROGRAM NO. 4

```
voltage doubler PWM CURRENT SOURCE ANALYSIS
*doubling rectifier fed by PWM current wave
* definition of the current source
iinl 1 0 pulse(0 1 1.11m 0.01m 0.01m 1.11m 20m)
iin2 1 0 pulse(0 1 3.33m 0.01m 0.01m 3.33m 20m)
iin3 1 0 pulse(0 1 7.77m 0.01m 0.01m 1.11m 20m)
iin4 1 0 pulse(0 -1 11.11m 0.01m 0.01m 1.11m 20m)
iin5 1 0 pulse(0 -1 13.33m 0.01m 0.01m 3.33m 20m)
iin6 1 0 pulse(0 -1 17.77m 0.01m 0.01m 1.11m 20m)
*source resistance
rs 1 7 1
* zero volts voltage source
vdo 7 8 0
*diodes and capacitors
dl 8 9 dl
cl 9 0 200u
c2 0 10 200u
d2 10 8 dl
*default model of the diode
rl 9 10 120
.model dl d
.options nopage
.tran 0.5m 140m
.plot tran v(9,10)
.plot tran i(vdo)
.end
```

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